OBJECTIVE 7–4 SECOND-ORDER CIRCUIT RESPONSES (SECTS. 7–5, 7–6, 7–7, 7–8)

Given one or more responses of a second-order *RLC* circuit:
(a) Find the circuit parameters or other responses.
(b) Design a circuit to produce a given response.
See Examples 7–16, 7–22 and Exercises 7–15, 7–16, 7–18

7–51 In a series *RLC* circuit the step response across the 4-μF capacitor is

$$v_C(t) = 14 - e^{-50t}[14\cos(350t) + 2\sin(350t)]\ \text{V} \qquad t \geq 0$$

(a) Find R and L.
(b) Find $i_L(t)$ for $t \geq 0$.

7–52 In a parallel *RLC* circuit the zero-input response in the 100-mH inductor is

$$i_L(t) = 50e^{-4000t} - 40e^{-5000t}\ \text{mA} \qquad t \geq 0$$

(a) Find R and C.
(b) Find $v_C(t)$ for $t \geq 0$.

7–53 In a parallel *RLC* circuit the state variable responses are

$$v_C(t) = e^{-100t}[5\cos(300t) + 15\sin(300t)]\ \text{V} \qquad t \geq 0$$

$$i_L(t) = 20 - 25e^{-100t}\cos(300t)\ \text{mA} \qquad t \geq 0$$

Find R, L, and C.

7–54 The zero-input response of a series *RLC* circuit with $R = 80\ \Omega$ is

$$v_C(t) = 2e^{-2000t}\cos(1000t) - 4e^{-2000t}\sin(1000t)\ \text{V} \qquad t \geq 0$$

If the initial conditions remain the same, what is the zero-input response when $R = 40\ \Omega$?

7–55 In a parallel *RLC* circuit the inductor current is observed to be

$$i_L(t) = 10e^{-10t}\cos(20t)\ \text{mA} \qquad t \geq 0$$

Find $v_C(t)$ when $v_C(0) = -10$ V.

7–56 D Design a parallel *RLC* circuit whose natural response has the form

$$v_L(t) = K_1e^{-2000t} + K_2e^{-3000t}\ \text{V} \qquad t \geq 0$$

7–57 D Design a series *RLC* circuit with $\zeta = 0.6$ and $\omega_0 = 4$ krad/s. What is the form of the natural response of $v_C(t)$ for your design?

7–58 D Design a series *RLC* circuit with $\zeta = 1$ and $\omega_0 = 10$ krad/s. What is the form of the natural response of $v_C(t)$ for your design?

7–59 The step response of a series *RLC* circuit is

$$v_C(t) = V_A - 2V_Ae^{-200t} + V_Ae^{-800t}\ \text{V} \qquad t > 0$$

where V_A is the amplitude of the input. What are the damping ratio and undamped natural frequency of the circuit?

7–60 What range of damping ratios is available in the circuit in Figure P7–60?

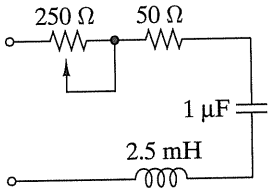

FIGURE P7–60

INTEGRATING PROBLEMS

7–61 A Reverse Step Response
The first-order *RC* circuit in Figure P7–61 is driven by a reverse step function input $v_S(t) = V_Au(-t)$. Derive an expression for $i_C(t)$ that is valid for $t \geq 0$.

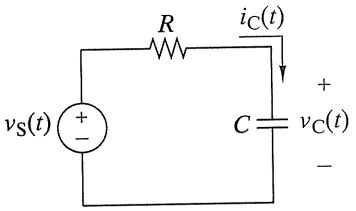

FIGURE P7–61

7–62 A First-Order OP AMP Circuit Step Response
Find the zero-state response of the OP AMP output voltage in Figure P7–62 when the input is $v_S(t) = V_Au(t)$.

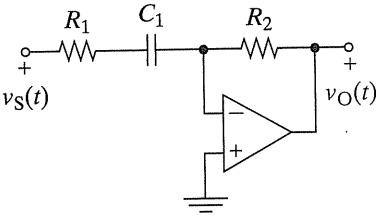

FIGURE P7–62

7–63 D *RC* Circuit Design
Design the first-order *RC* circuit in Figure P7–63 so an input $v_S(t) = 10u(t)$ V produces a zero-state response $v_O(t) = 10 - 5e^{-500t}$ V.

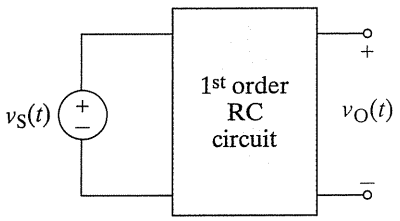

FIGURE P7–63

7–64 D Sample Hold Circuit

Figure P7–64 is a simplified diagram of a sample hold circuit. When the switch is in position A, the circuit is in the sample mode and the capacitor voltage must charge to at least 99% of the source voltage V_A in less than 1 μs. When the switch is moved to position B, the circuit is in the hold mode and the capacitor must retain at least 99% of V_A for at least 1 ms. Select a capacitance that meets these constraints.

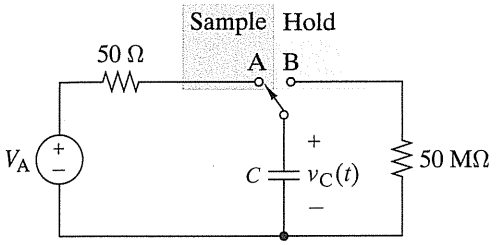

FIGURE P7–64

7–65 A Supercapacitor

Supercapacitors have very large capacitance (typically from 0.1 to 50 F), small sizes, and very long charge holding times, making them useful in nonbattery backup power applications. The charge holding quality of a supercapacitor is measured using the circuit in Figure P7–65. The switch is closed for a long time (say, 24 hours) and the capacitor is charged to 5 V. The switch is then opened and the capacitor allowed to self-discharge through any leakage resistance for 24 hours. Suppose that after 24 hours the voltage across a 0.47-F supercapacitor is 4.5 V. What is the equivalent leakage resistance in parallel with the capacitor?

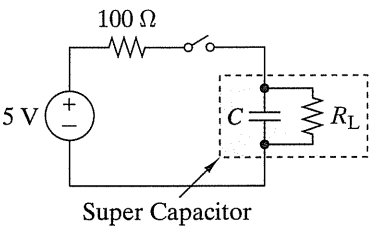

FIGURE P7–65

7–66 A Obtaining a Critically Damped Response

The voltage across a 500-Ω resistor in a series *RLC* circuit is $v_R(t) = 10e^{-500t}\sin(3500t)$ V. How much additional resistance is needed for the response to be critically damped?

7–67 A Combined First- and Second-Order Response

The switch in Figure P7–67 has been in position A for a long time and is moved to position B at $t = 0$ and then to position C when $t = 10$ ms. For $0 < t < 10$ ms the capacitor voltage is a charging exponential $v_C(t) = 10(1 - e^{-100t})$ V. For $t > 10$ ms the capacitor voltage is a sinusoid $v_C(t) = 6.321\cos[1000(t - 0.1)]$ V.

(a) Suppose the resistance is reduced to 1 kΩ and the switching sequence repeated. Will the amplitude of the sinusoid increase, decrease, or stay the same? Will the frequency of the sinusoid increase, decrease, or stay the same?

(b) Suppose the inductance is reduced to 100 mH and the switching sequence repeated. Will the amplitude of the sinusoid increase, decrease, or stay the same? Will the frequency of the sinusoid increase, decrease, or stay the same?

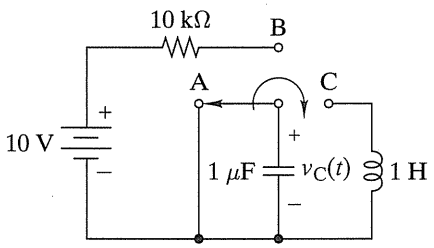

FIGURE P7–67

7–68 A Second-Order *RC* Circuit

Find the second-order differential equation relating v_O and i_S in Figure P7–68.

Hint: Write node-voltage equations.

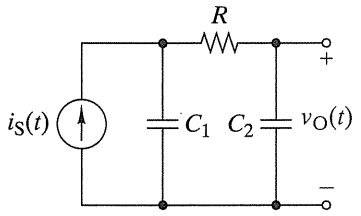

FIGURE P7–68

7–69 D Lightning Pulser Design

The circuit in Figure P7–69 is a simplified diagram of a pulser that delivers simulated lightning transients to the test article at the output interface. Closing the switch must produce a short-circuit current of the form $i_{SC}(t) = I_A e^{-\alpha t}\cos(\beta t)$, with $\alpha = 100$ krad/s, $\beta = 200$ krad/s, and $I_A = 2$ kA. Select the values of L, C, and V_0.

8–4 Use the phasors in Problem 8–3 and the additive property to find the sinusoidal waveforms $2v_1(t) + v_2(t)$ and $i_1(t) + 3i_2(t)$.

8–5 The phasor representation of a sinusoid with $\omega = 25$ rad/s is $\mathbf{V} = 15 + j10$ V. Use the phasor derivative property to find the time derivative of the sinusoid.

8–6 Convert the following phasors into sinusoids:

(a) $\mathbf{V}_1 = 20 + j25$ V, $\omega = 10$ rad/s

(b) $\mathbf{V}_2 = (8 - j3)5$ V, $\omega = 20$ rad/s

(c) $\mathbf{I}_1 = 12 - j5 + \dfrac{4}{j}$ A, $\omega = 300$ rad/s

(d) $\mathbf{I}_2 = \dfrac{3 + j8}{2 - j6}$ A, $\omega = 50$ rad/s

8–7 Use phasors to find the sinusoid $v_2(t)$, where

$$v_2(t) = \frac{1}{10}\frac{dv_1(t)}{dt} + 20\,v_1(t) \quad \text{and} \quad v_1(t) = 10\cos(250t + 90°)$$

8–8 Given the sinusoids

$$v_1(t) = 50\cos(\omega t - 45°) \quad \text{and} \quad v_2(t) = 25\sin(\omega t)$$

use the additive property of phasors to find $v_3(t)$ such that $v_1 + v_2 + v_3 = 0$.

8–9 Use phasors to find the sinusoid $v_1(t)$, where

$$\frac{dv_1(t)}{dt} + 250v_1(t) = 50v_2(t) \quad \text{and} \quad v_2(t) = 5\cos(100t)$$

8–10 Given a sinusoid $v_1(t)$ whose phasor is $\mathbf{V}_1 = -3 + j4$ V, use phasor methods to find the voltage $v_2(t)$ that leads $v_1(t)$ by 90° and has an amplitude of 10 V.

OBJECTIVE 8–2 EQUIVALENT IMPEDANCE (SECTS. 8–2, 8–3)

Given a linear circuit, use series and parallel equivalence to find the equivalent impedance at a specified pair of terminals. See Examples 8–5, 8–6, 8–9, 8–10, 8–12 and Exercises 8–8, 8–10, 8–11

8–11 Find the equivalent impedance Z in Figure P8–11 when $\omega = 1000$ rad/s. Express the result in both polar and rectangular form.

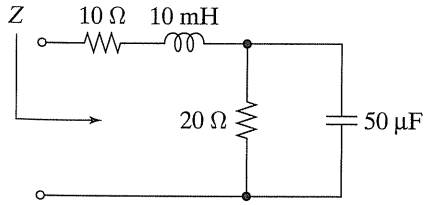

FIGURE P8–11

8–12 Find the equivalent impedance Z in Figure P8–12. Express the result in both polar and rectangular form.

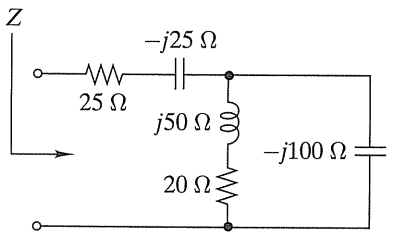

FIGURE P8–12

8–13 Find the equivalent impedance Z in Figure P8–13 when $\omega = 10$ krad/s. Express the result in both polar and rectangular form.

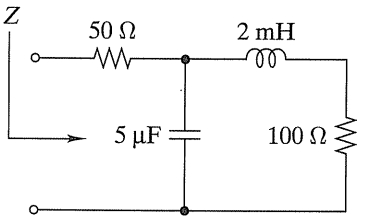

FIGURE P8–13

8–14 Find the equivalent impedance Z in Figure P8–14. Express the result in both polar and rectangular form.

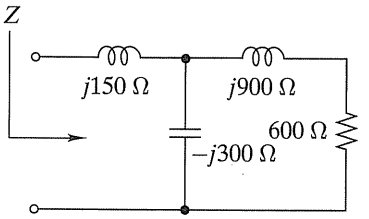

FIGURE P8–14

8–15 The circuit in Figure P8–14 is operating in the sinusoidal steady state with $\omega = 3$ krad/s. How would the element impedances change if the steady-state frequency is reduced to 1 krad/s? What is the equivalent impedance Z at this new frequency?

8–27 The circuit in Figure P8–27 is operating in the sinusoidal steady state. Find the steady-state response $v_x(t)$.

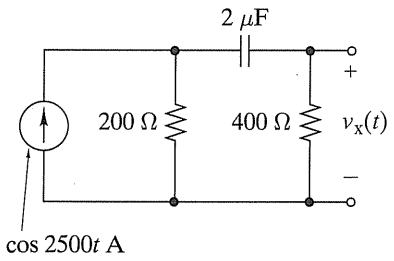

FIGURE P8–27

8–28 The circuit in Figure P8–28 is operating in the sinusoidal steady state. Find the steady-state phasor response $\mathbf{V}_x$.

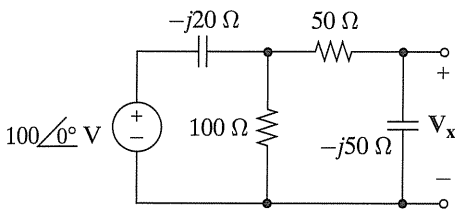

FIGURE P8–28

8–29 The circuit in Figure P8–29 is operating in the sinusoidal steady state. Use superposition to find the phasor response $\mathbf{I}_x$.

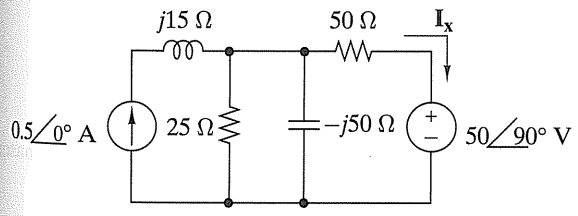

FIGURE P8–29

8–30 The circuit in Figure P8–30 is operating in the sinusoidal steady state. Use superposition to find the response $v_x(t)$. *Note:* The sources do not have the same frequency.

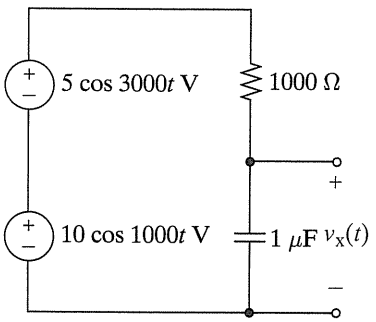

FIGURE P8–30

8–31 The circuit in Figure P8–31 is operating in the sinusoidal steady state. Use superposition to find the response $v_x(t)$. *Note:* The sources do not have the same frequency.

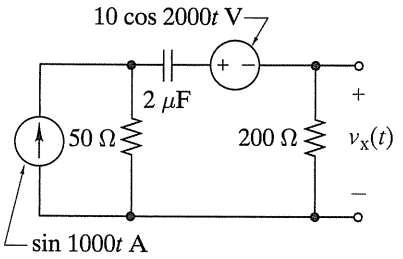

FIGURE P8–31

8–32 The circuit in Figure P8–32 is operating in the sinusoidal steady state. Find the phasor response $\mathbf{V}_x$.

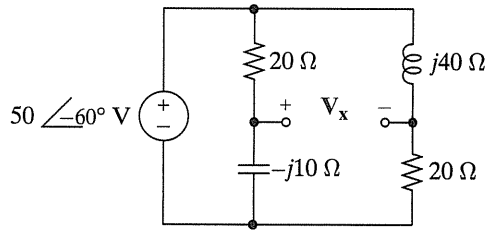

FIGURE P8–32

8–33 The circuit in Figure P8–33 is operating in the sinusoidal steady state. Use the unit output method to find the phasor response $\mathbf{V}_x$.

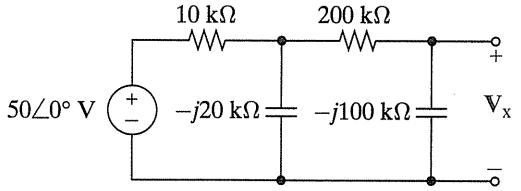

FIGURE P8–33

8–43 Find the node voltage phasors $\mathbf{V}_A$ and $\mathbf{V}_B$ in Figure P8–43.

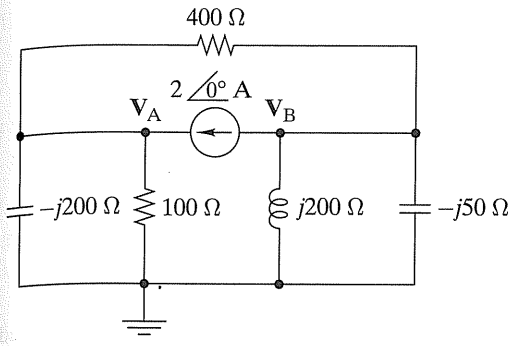

FIGURE P8–43

8–44 Use mesh-current analysis to find the phasor branch currents $\mathbf{I}_1$, $\mathbf{I}_2$, and $\mathbf{I}_3$ in the circuit shown in Figure P8–44.

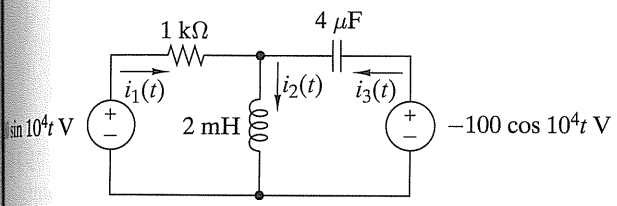

FIGURE P8–44

8–45 Use mesh-current to find the phasor currents $\mathbf{I}_A$ and $\mathbf{I}_B$ in Figure P8–45.

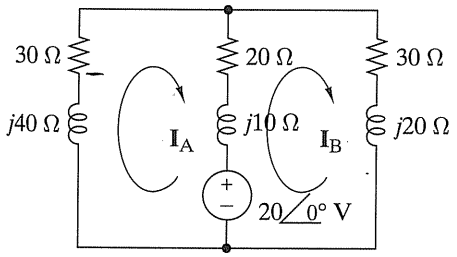

FIGURE P8–45

8–46 Use mesh-current analysis to solve Problem 8–42.

8–47 Find the phasor current $\mathbf{I}_O$ in Figure P8–47.

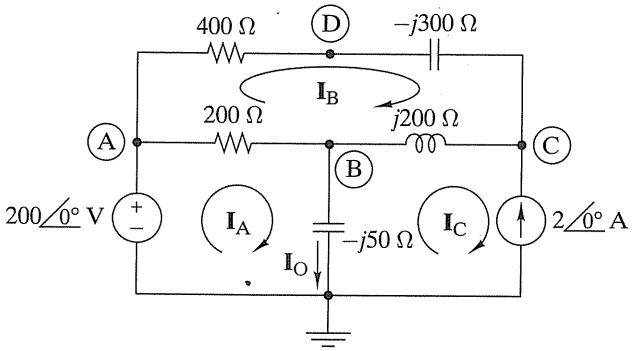

FIGURE P8–47

8–48 Find the phasor outputs $\mathbf{V}_O$ and $\mathbf{I}_O$ in Figure P8–48 when $\mu = 10$ and the phasor input is $\mathbf{I}_S = 1 + j0$ mA.

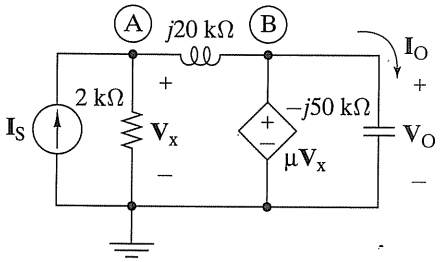

FIGURE P8–48

8–49 Find the phasor responses $\mathbf{I}_{IN}$ and $\mathbf{V}_O$ in Figure P8–49 when $\mathbf{V}_S = 1 + j0$ V.

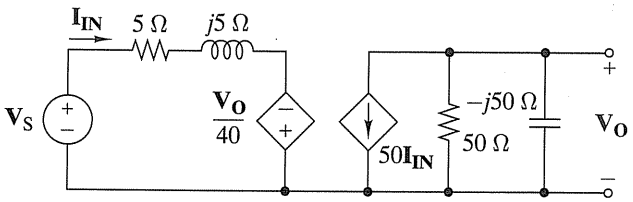

FIGURE P8–49

8–50 The OP AMP circuit in Figure P8–50 is operating in the sinusoidal steady state with $\omega = 100$ krad/s. Find the phasor input $\mathbf{V}_S$ when the phasor output is $\mathbf{V}_O = 10 + j0$ V.