

# Ask the Applications Engineer—30

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## PLL SYNTHESIZERS

*Q. What is a PLL Synthesizer?*

A. A frequency synthesizer allows the designer to generate a variety of output frequencies as multiples of a single reference frequency. The main application is in generating local oscillator (LO) signals for the up- and down-conversion of RF signals.

The synthesizer works in a *phase-locked loop* (PLL), where a phase/frequency detector (PFD) compares a fed back frequency with a divided-down version of the reference frequency (Figure 1). The PFD's output current pulses are filtered and integrated to generate a voltage. This voltage drives an external voltage-controlled oscillator (VCO) to increase or decrease the output frequency so as to drive the PFD's average output towards zero.

Frequency is scaled by the use of counters. In the example shown, an ADF4xxx synthesizer is used with an external filter and VCO. An input reference (R) counter reduces the reference input frequency (13 MHz in this example) to PFD frequency ( $F_{PFD} = F_{REF}/R$ ); and a feedback (N) counter reduces the output frequency for comparison with the scaled reference frequency at the PFD. At equilibrium, the two frequencies are equal, and the output frequency is  $N \times F_{PFD}$ . The feedback counter is a *dual-modulus prescaler type*, with A and B counters ( $N = BP + A$ , where P is the prescale value).

Figure 2 shows a typical application in a superheterodyne receiver. Base station and handset LOs are the most common application, but synthesizers are also found in low frequency clock generators (ADF4001), wireless LANs (5.8 GHz), radar systems, and collision-avoidance systems (ADF4106).

*Q. What are the key performance parameters to be considered in selecting a PLL synthesizer?*

A. The major ones are: phase noise, reference spurs, and lock time.

**Phase Noise:** For a carrier frequency at a given power level, the phase noise of a synthesizer is the ratio of the carrier power

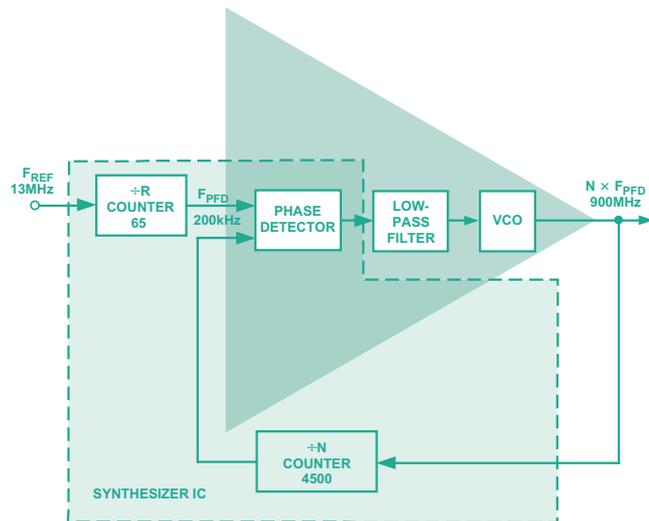


Figure 1. Block diagram of a PLL.

to the power found in a 1-Hz bandwidth at a defined frequency offset (usually 1 kHz for a synthesizer). Expressed in dBc/Hz, the in-band (or close-in) phase noise is dominated by the synthesizer; the VCO noise contribution is high-pass filtered in the closed loop.

**Reference Spurs:** These are artifacts at discrete offset frequencies generated by the internal counters and charge pump operation at the PFD frequency. These spurs will be increased by mismatched up and down currents from the charge pump, charge-pump leakage, and inadequate decoupling of supplies. The spurious tones will get mixed down on top of the wanted signal and decrease receiver sensitivity.

**Lock Time:** The lock time of a PLL is the time it takes to jump from one specified frequency to another specified frequency within a given frequency tolerance. The jump size is normally determined by the maximum jump the PLL will have to accomplish when operating in its allocated frequency band. The step-size for GSM-900 is 45 MHz and for GSM-1800 is 95 MHz. The required frequency tolerances are 90 Hz and 180 Hz, respectively. The PLL must complete the required frequency step in less than 1.5 time slots, where each time slot is 577  $\mu$ s.

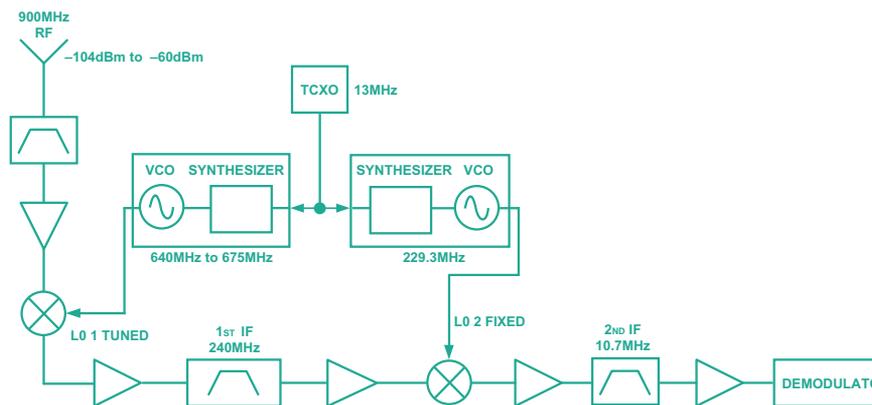


Figure 2. Dual PLL used to mix down from GSM RF to baseband.

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**Q.** I've selected my synthesizer based on the output frequency required. What about choosing the other elements in the PLL?

**A.** **Frequency Reference:** A good, high quality, low-phase-noise reference is crucial to a stable low-phase-noise RF output. A square wave or clipped sine wave available from a TCXO crystal offers excellent performance, because the sharper clocking edge results in less phase jitter at the R-counter output. The ADF4206 family features on-board oscillator circuitry allowing low cost AT-cut crystals to be used as the reference. While predictable AT crystals cost one third as much as TCXOs, their temperature stability is poor unless a compensation scheme with a varactor is implemented.

**VCO:** The VCO will convert the applied tuning voltage to an output frequency. The sensitivity can vary drastically over the full frequency range of the VCO. This may make the loop unstable (see *loop filter*). In general, the lower the tuning sensitivity ( $K_v$ ) of the VCO, the better the VCO phase noise will be. The synthesizer phase noise will dominate at smaller offsets from the carrier. Farther away from the carrier, the high-pass-filtered noise of the VCO will begin to dominate. The GSM specification for out-of-band phase noise is  $-130$  dBc/Hz at a 1-MHz offset.

**Loop Filter:** There are many different types of loop filter. The most common is the third-order integrator shown in Figure 3. In general, the loop filter bandwidth should be 1/10 of the PFD frequency (channel spacing). Increasing the loop bandwidth will reduce the lock time, but the filter bandwidth should never be more than PFD/5, to avoid significantly increasing the risk of instability.

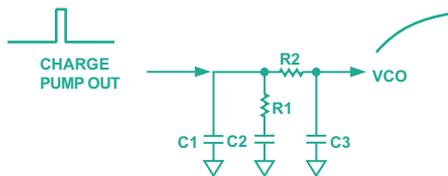


Figure 3. A third-order loop filter. The R2C3 pole provides extra attenuation for spurious products.

A loop filter's bandwidth can be doubled by doubling either the PFD frequency or the charge-pump current. If the actual  $K_v$  of the VCO is significantly higher than the nominal  $K_v$  used to design the loop filter, the loop bandwidth will be significantly wider than expected. The variation of loop bandwidth with  $K_v$  presents a major design challenge in wideband PLL designs, where the  $K_v$  can vary by more than 300%. Increasing or decreasing the programmable charge-pump current is the easiest way to compensate for changes in the loop bandwidth caused by the variation in  $K_v$ .

**Q.** How do I optimize PLL design for phase noise?

**A.** **Use low N-value:** Since phase noise is multiplied up from the PFD (reference frequency) at a rate of  $20 \log N$ , reducing  $N$  by a factor of 2 will improve system phase noise by 3 dB (i.e., doubling the PFD frequency reduces phase noise by  $10 \log 2$ ). Therefore the highest feasible PFD frequency should always be used.

**Choose a higher frequency synthesizer than is required:** Operating under the same conditions at 900 MHz, the ADF4106 will give 6-dB better phase noise than the ADF4111 (see Table 1).

Use the lowest Rset resistor specified for operation: Reducing the Rset increases the charge-pump current, which reduces phase noise.

**Table 1. The integrated phase jitter depends heavily on the in-band phase noise of the synthesizer. System parameters: [900-MHz RF, 200-kHz PFD, 20-kHz loop filter]**

Synthesizer Model	In-Band Phase Noise (dB)	Integration Range (Hz)	Integrated Phase Error Degrees rms
ADF4111	-86	100 to 1 M	0.86
ADF4112	-89	100 to 1 M	0.62
ADF4113	-91	100 to 1 M	0.56
ADF4106	-92.5	100 to 1 M	0.45

**Q.** Why is phase noise important?

**A.** Phase noise is probably the most crucial specification in PLL selection. In a *transmit* chain, the linear power amplifier (PA) is the most difficult block to design. A low-phase-noise LO will give the designer greater margin for non-linearity in the PA by reducing the phase error in the up-conversion of the baseband signal.

The system maximum phase error specification for GSM receivers/transmitters (Rx/Tx) is  $5^\circ$  rms. As one can see in Table 1, the allowable PA phase-error contribution can be significantly greater when the phase noise contributed by the PLL is reduced.

On the receive side, low phase noise is crucial to obtaining good receiver selectivity (the ability of the receiver to demodulate signals in the presence of interferers). In the example of Figure 4, on the left the desired low level signal is swamped by a nearby undesired signal mixing with the LO noise (enclosed dashed area). In this case the filters will be unable to block these unwanted interferers. In order to demodulate the desired RF signal, either the transmit side will require higher output power, or the LO phase noise will need to be improved.

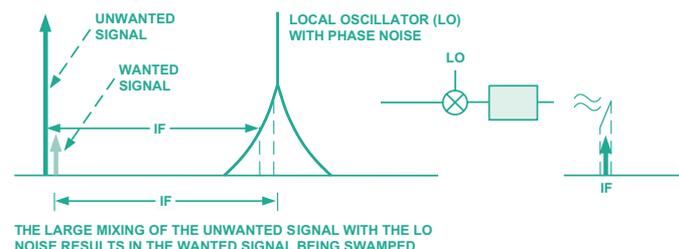


Figure 4. A large unwanted signal mixing with LO noise swamps the wanted signal. Increased phase noise will reduce the sensitivity of the receiver, since the demodulator will not be able to resolve the signal from the noise.

**Q.** Why are spur levels important?

**A.** Most communication standards will have stringent maximum specifications on the level of spurious frequency components (*spurs*) that the LO can generate. In *transmit* mode, the spur levels must be limited to ensure that they do not interfere with users in the same or a nearby system. In a *receiver*, the LO spurs

can significantly reduce the ability to demodulate the mixed-down signal. Figure 4 shows the effect of reciprocal mixing where the desired signal is swamped with noise due to a large undesired signal mixing with noise on the oscillator. The same effect will occur for spurious noise components.

A high level of spurs can indirectly affect lock time by forcing the designer to narrow the loop bandwidth—slowing response—in order to provide sufficient attenuation of these unwanted components. The key synthesizer specifications to ensure low reference spurs are *low charge-pump leakage* and *matching of the charge pump currents*.

**Q. Why is lock time important?**

A. Many systems use frequency hopping as a means to protect data security, avoid multi-path fading, and avoid interference. The time spent by the PLL in achieving frequency lock is valuable time that cannot be used for transmitting or receiving data; this reduces the effective data rate achievable. Currently there is no PLL available that can frequency-hop quickly enough to meet the timing requirements of the GSM protocol. In base-station applications, two separate PLL devices are used in parallel to reduce the number of wasted slots. While the first is generating the LO for the transmitter, the second PLL is moving to the next allocated channel. In this case a super-fast (<10-μs) settling PLL would significantly reduce the bill of materials (BOM) and layout complexity.

**Q. How do I minimize lock time?**

A. By increasing the PFD frequency. The PFD frequency determines the rate at which a comparison is made between the VCO/N and the reference signal. Increasing the PFD frequency increases the update of the charge pump and reduces lock time. It also allows the loop bandwidth to be widened.

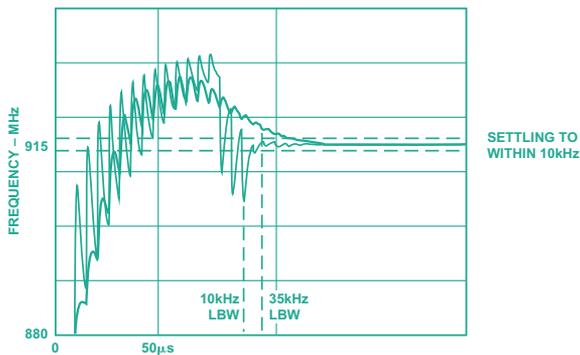


Figure 5. Loop bandwidth has a significant effect on the lock time. The wider the loop bandwidth, the faster the lock time, but also the greater the level of spurious components. Lock time to 1 kHz is 142 μs with a 35-kHz LBW—and 248 μs with a 10-kHz LBW.

**Loop Bandwidth.** The wider the loop bandwidth, the faster the lock time. The trade-off is that a wider loop bandwidth will reduce attenuation of spurious products and increase the integrated phase noise. Increasing the loop bandwidth significantly (>PFD/5) may cause the loop to become unstable and permanently lose lock. A phase margin of 45 degrees produces the optimum settling transient.

**Avoid tuning voltages nearing ground or Vp.** When the tuning voltage is within a volt of the rails of the charge pump supply (Vp), the charge pump begins to operate in a saturation region.

Operation in this region will degrade settling time significantly; it may also result in mismatch between jumping-up in frequency and jumping down. Operation in this saturation region can be avoided by using the maximum Vp available or using an active loop filter. Using a VCO with a higher Kv will allow Vtune to remain closer to Vp/2 while still tuning over the required frequency range.

**Choose plastic capacitors.** Some capacitors exhibit a dielectric memory effect, which can impede lock time. For fast phase locking applications ‘plastic-film’ Panasonic ECHU capacitors are recommended.

**Q. What factors determine the maximum PFD frequency I can use?**

A. In order to obtain contiguous output frequencies in steps of the PFD frequency

$$F_{PFD} < \frac{V_{CO} \text{ Output Frequency}}{(P^2 - P)}$$

where P is the prescaler value.

The ADF4xxx offers prescaler selections as low as 8/9. This permits a higher PFD frequency than many competitive parts, without violating the above rule—enabling lower phase noise PLL design. Even if this condition is not met, the PLL will lock if  $B > A$  and  $B > 2$  in the programming registers.

**Q. Fractional-N has been around since 1970. What are its advantages to PLL designers?**

A. The resolution at the output of an integer-N PLL is limited to steps of the PFD frequency. Fractional-N allows the resolution at the PLL output to be reduced to small fractions of the PFD frequency. It is possible to generate output frequencies with resolutions of 100s of Hz, while maintaining a high PFD frequency. As a result the N-value is significantly less than for integer-N. Since noise at the charge pump is multiplied up to the output at a rate of  $20 \log N$ , significant improvements in phase noise are possible. For a GSM900 system, the fractional-N ADF4252 offers phase noise performance of -103 dBc/Hz, compared with -93 dBc/Hz for the ADF4106 integer-N PLL.

Also offering a significant advantage is the lock-time improvement made possible by fractional-N. The PFD frequency set to 20 MHz and loop bandwidth of 150 kHz will allow the synthesizer jump 30 MHz in <30 μs. Current base stations require 2 PLL blocks to ensure that LOs can meet the timing requirements for transmissions. With the super-fast lock times of fractional-N, future synthesizers will have lock time specs that allow the 2 “ping-pong” PLLs to be replaced with a single fractional-N PLL block.

**Q. If fractional-N offers all these advantages, why are integer-N PLLs still so popular?**

A. Spurious levels! A fractional-N divide by 19.1 consists of the N-divider dividing by nineteen 90% of the time, and by twenty 10% of the time. The average division is correct, but the instantaneous division is incorrect. Because of this, the PFD and charge pump are constantly trying to correct for instantaneous phase errors. The heavy digital activity of the sigma-delta modulator, which provides the averaging function, creates spurious components at the output. The

digital noise, combined with inaccuracies in matching the hard-working charge pump, results in spurious levels greater than those allowable by most communications standards. Only recently have fractional-N parts, such as the ADF4252, made the necessary improvements in spurious performance to allow designers to consider their use in traditional integer-N markets.

**Q.** *What PLL devices have you released recently, how do they differ, and where would I use them?*

**A.** **ADF4001** is a <200-MHz PLL, pin-compatible with the popular ADF4110 series, but with the prescaler removed. Applications are stable reference clock generators, in cases where all clocks must be synchronized with a single reference source. They are generally used with VCXOs (voltage-controlled crystal oscillators), which have lower gain (Kv) and better phase noise than VCOs.

**ADF4252** is a dual fractional-N device with <70 dBc spurious. It offers <20- $\mu$ s lock times vs. 250  $\mu$ s for integer-N, with <100 dBc/Hz phase noise due to the high PFD frequency—a ground-breaking product with a software-programmable trade-off between phase noise and spurs.

**ADF4217L/ADF4218L/ADF4219L** are low-phase-noise upgrades for the LMX2331L/LMX2330L/LMX2370. They consume only 7.1 mA, with a 4-dB improvement in phase noise over competitive devices. Great news for handset designers!

**ADF4106** is a 6-GHz PLL synthesizer. Ideal for WLAN equipment in the 5.4-to-5.8-GHz frequency band, it is the lowest-noise integer-N PLL on the market.

**Q.** *What tools are available to simulate loop behavior?*

**A.** ADIsimPLL is a simulation tool developed with Applied Radio Labs. It consists of extensive models for the ADI synthesizers as well as popular VCOs and TCXOs. It allows the user to design passive and active loop filters in many configurations, simulate VCO, PLL, and reference noise, and model spurious and settling behavior. Once a design is completed, a custom evaluation board may be ordered based on the design using an internal weblink to Avnet.

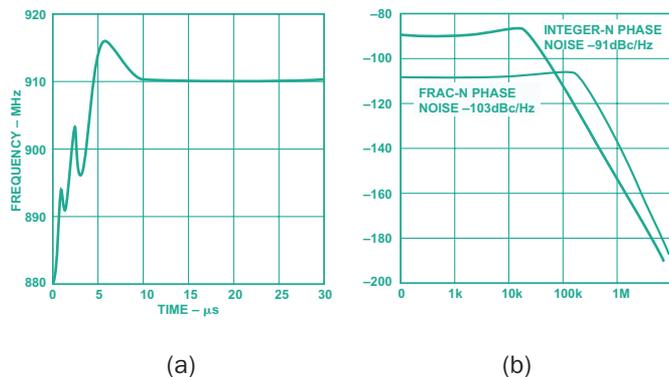


Figure 6. Lock time and phase noise are just two parameters that can be modeled by ADIsimPLL. While phase noise is reduced by >8 dB, the wider loop bandwidths and high PFD frequency allowed by fractional-N reduce the lock time to <30  $\mu$ s for 30-MHz jumps (as shown).

The tool is free and may be downloaded from [www.analog.com/pll](http://www.analog.com/pll). Also widely used are the commercially available Eagleware and MATLAB tools.

**Q.** *Do ADI proprietary parts have specific advantages over comparable competitive parts?*

**A.** Phase noise is the critical specification for many system designers. Phase-noise performance in the ADF4113 family is typically 6 dB better than the National equivalent and >10 dB better than Fujitsu or Philips equivalents. The extended choice of prescaler settings protects the designer from being compromised in selecting a higher PFD frequency by the ‘ $P^2 - P$ ’ rule. Another major advantage is the choice of eight programmable charge-pump currents; in wideband designs where the gain of the VCO changes dramatically, the programmable currents can be adjusted to ensure loop stability and bandwidth consistency across the entire band.

**Q.** *What is the future direction of the PLL industry?*

**A.** While chipset solutions are prominent in the headlines, particularly for GSM, the new generation of cellular phone and base stations are still likely to initially favor discrete solutions. Discrete PLL and VCO modules offer improved noise performance and isolation, and are already in high volume production at the start of the design cycle.

The demand for reduced size and current consumption in handsets has driven the development of the ADI L-series of dual synthesizers on 0.35- $\mu$ m Bi-CMOS in miniature CSP packages. Integrated VCO and PLL modules will be a major growth in newer system designs, where board area and cost reduction of an initial design is crucial.

However the most exciting developments are likely to be in fractional-N technology. Recent improvements in spur performance have allowed the release of the ADF4252 and created unprecedented interest. The phase-noise improvement, super-fast lock times, and versatility inherent in the architecture are likely to dominate LO blocks of future multi-standard high-data-rate wireless systems.

### Acknowledgements

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