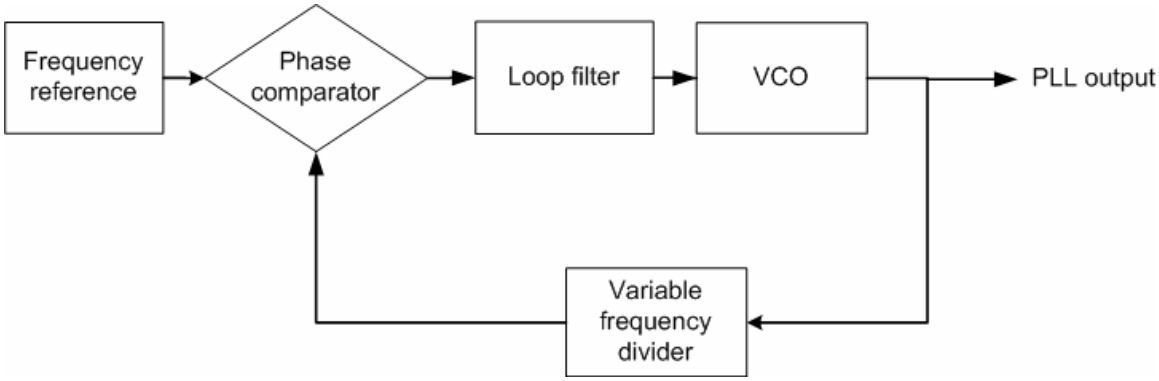
EEE411/EEE511 LAB # 8

PLL Frequency Synthesizer

In this experiment you will design and construct a PLL (Phase-Locked Loop) frequency synthesizer using the VCO you have designed and constructed at the previous experiment and ADF4001 frequency syhntesizer chip from analog devices. The block diagram of the synthesizer is shown below. You are going to get the frequency reference from your signal generator back panel. The reference frequency output of the signal generator is your frequency reference. VCO is the VCO that you have constructed yourself. Phase comparator and the variable frequency divider are inside the ADF4001 chip. At this preliminary work you are going to design the PLL by designing the Loop Filter.



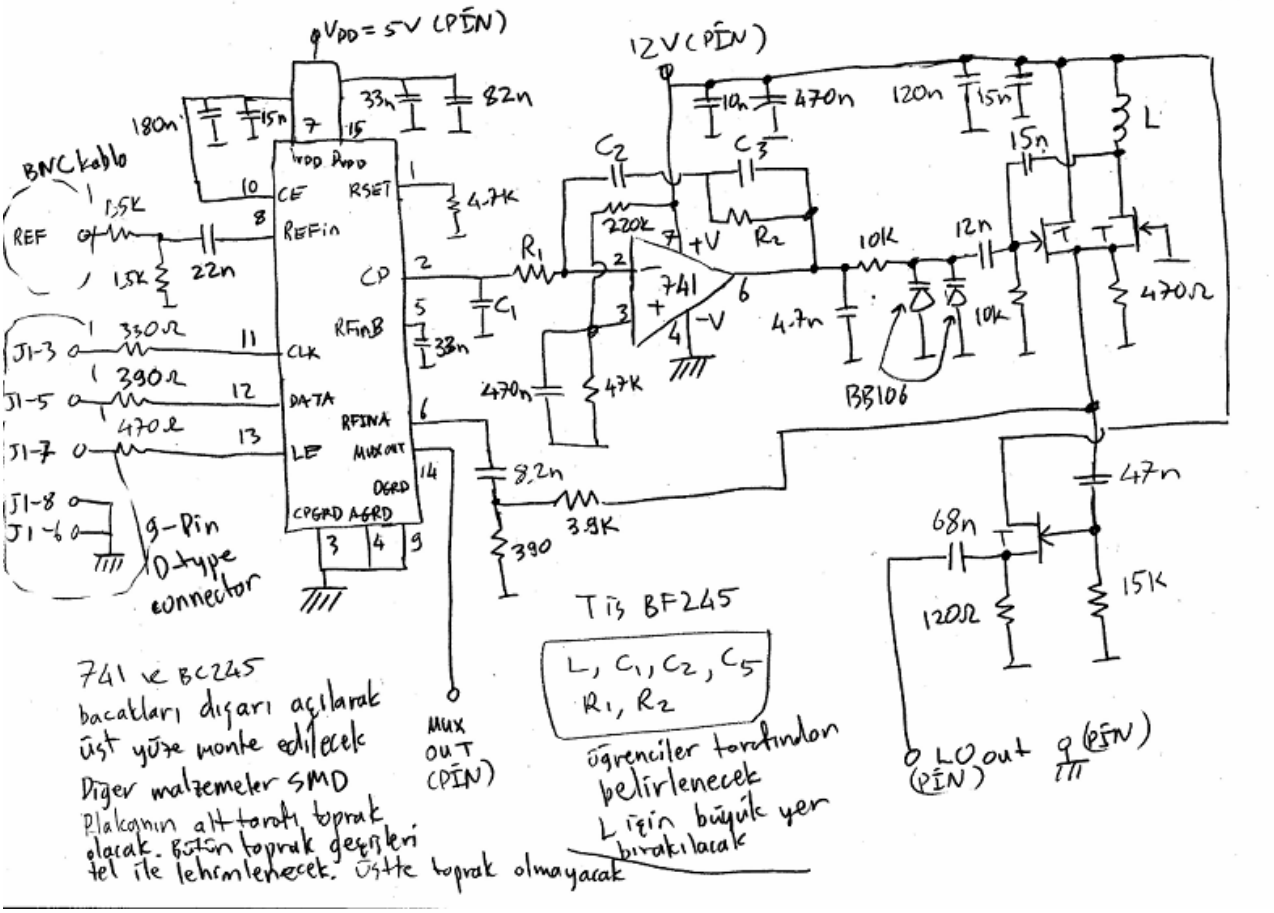
Block diagram of PLL

The specification of the PLL frequency synthesizer is given below:

1. Channel spacing is 50 kHz.
2. Output reference spur should be less than 60 dBc.
3. Lock time must be less than 10 msec (time to converge into 1 Hz)
4. Output frequency range is 44.3 +/-1 MHz.
5. Output power is in the range 0 to 10 dBm.

Preliminary Work:

1. Design the PLL by designing the loop filter. The circuit diagram of the PLL is given below.



You need to design the loop filter of the PLL by using ADISIMPLL which can be downloaded from the web page of "analog devices" . Analog devices is the manufacturer of the PLL chip ADF4001. The program gives you the values of the components C_1, C_2, C_3, R_1 and R_2 if you configure it properly. Opamp positive input is biased to 2.5 Volts approximately in order to give the charge pump enough voltage range to operate properly. The 470nF capacitor is used to filter out interference and noise from the positive input of the opamp.

2. Study the data sheet of the PLL chip ADF4001 very carefully.
3. Learn how to program the chip. Download the program which configures the PLL chip from the analog devices web site and try to use it.

Lab Work:

1. Construct the rest of the circuit also using the components you have designed yourself. Cnnect the reference from the signal generator. Monitor the output using your scope and use the scope for measuring the output frequency.
2. Open the driver software for commanding the PLL. Check if the PLL creates the range of frequencies by changing the synthesized frequency in the operating frequency range.
3. Measure the lock time of the synthesizer by monitoring the VCO input by the oscilloscope.
4. Repeat the same thing by monitoring the MUX output of the synthesizer.
5. Monitor the output by using a spectrum analyser to see if there are any spurious signals. Measure the spurious signal levels if you can find any. Also measure the frequency of operation by using the spectrum analyser.

Discussion:

Comment on the lock time measurements. Are there any differences between the lock time measurements? How precise is the output frequency of the synthesizer?