# EEE411-511 EXP3

Experiment:

This experiment is about building a tuned IF amplifier including a ceramic IF filter. The circuit diagram of the amplifier is shown below. The amplifier is based on BF245C transistor. It is designed around the cascode concept in order to prevent unnecessary oscillations. 2.2 kΩ at the drain is used to control drain impedance in order not to let the circuit to oscillate.
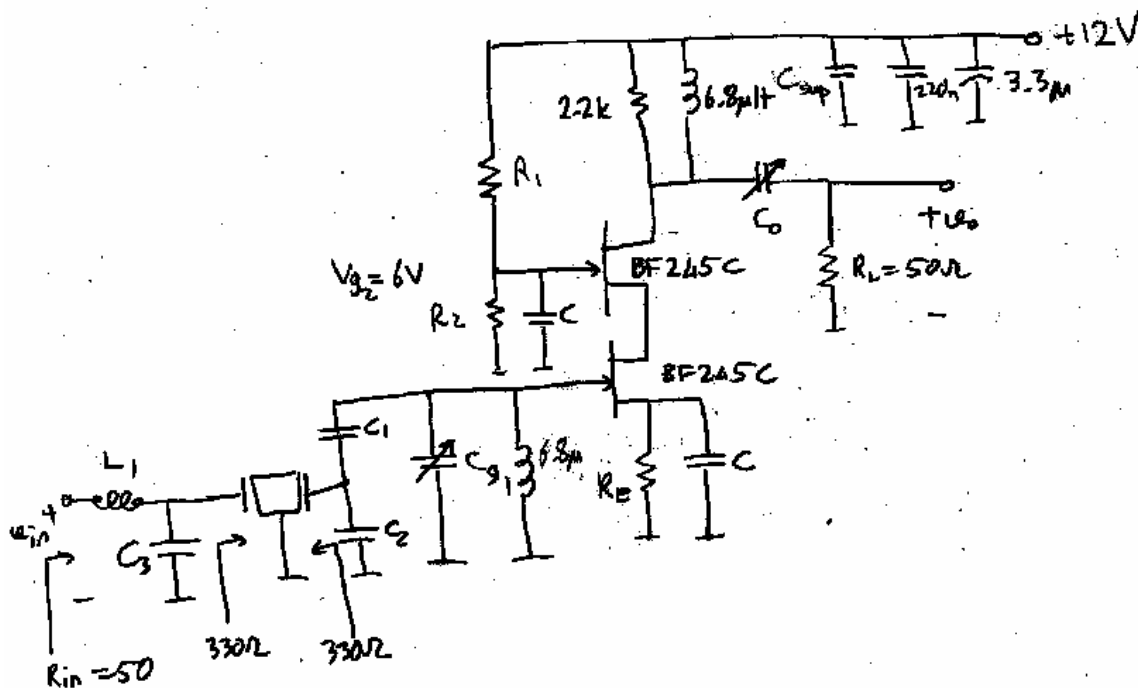
Preliminary work:

1. Start the design by finding a suitable power supply decoupling capacitor (Csup), suitable source degenaration capacitor (C), and the gate shunt capacitor C (Hint choose the capacitors to be at self resonance at the IF frequency, please take notice that typically 1nH leaded capacitor resonates at 150 MHz).
2. Bias the gate of the second transistor (G2) to 6 Volts DC by choosing the resistors R_1 end R_2.
3. Using the data sheet of BC245C find a suitable bias current for the transistors (The higher the transconductance, the better). Choose a suitable bias resistor R_E.

4. The input and output impedances of the IF filter is 330 Ω. They must also be terminated by the same impedance. The diagram of the IF filter is shown below. Match the input impedance of the amplifier to 50 Ω using the L-match shown.
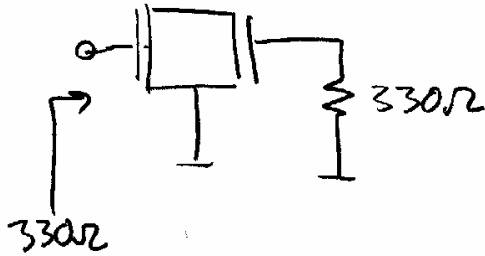
5. Check the input impedance (gate-to-source impedance) of BC245C. Find the values of C_1 and C_2 and C_{g1} in order to deliver maximum power to the input of the transistor (The available variable capacitor at the lab is 7-35 pF.
6. Find the value of Co in order to match the 50 Ω to the drain, to that maximum power is transferred to the load.
7. Plot the gain of the amplifier versus frequency using Spice simulation.

While carrying out the preliminary work, please note that the Q of the 6.8 μH that we are going to use at the lab at 10.7 MHz is about 40.

Experiment:

1. Construct your circuit step-by-step, measuring your circuit at each step shown below:
    a. Construct the L-match of the IF filter, load the other end by 330 Ω and measure and plot the input impedance on smith chart using the network analyser.
    b. Add the components, C_1 and C_2, C_{g1} and 6.8 μH, measured the impedance driving the gate of the first transistor at the network analyser.
    c. Determine the value of Csup by measuring various the impedance of ceramic capacitors with shortest leads using a network analyser.
    d. Construct the rest of the circuit
    e. Check the DC biases and correct the cicuit if necessary to make the circuit work properly.
    f. Connect a signal generator to the input of the circuit using a 50 Ω cable and monitor the output using an oscilloscope.
    g. Adjust the capacitors for maximum gain.
    h. Measure the input impedance of the amplifier against frequency and plot using the network analyser.
2. Connect a 50 Ω cable to the output of the circuit, too, and measure the gain of the circuit against frequency using the network analyser.
3. Measure the group delay of the amplifier using the network analyser

Measure the input impedance of the IF filter using a network analyser.

Results:

1. What is the 3 dB bandwith of the amplifier?
2. What is the group delay distortion of the amplifier in that BW?
3. What is the maximum symbol rate that this amplifier can support without problems?
4. What is the voltage gain of the amplifier in dB's?
5. What is the power gain of the amplifier in dB's?
6. Comment on the difference.

Spice model of BF245C:

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*
.MODEL BF245C/PLP NJF
+        VTO = -5.0014E+000
+        BETA = 5.43157E-004
+        LAMBDA = 2.71505E-002
+         RD = 1.20869E+001
+         RS = 1.20869E+001
+         IS = 3.64346E-016
+        CGS  = 2.00000E-012
+        CGD  = 2.00000E-012
+         PB = 1.24659E+000
+         FC = 5.00000E-001
*
*$
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