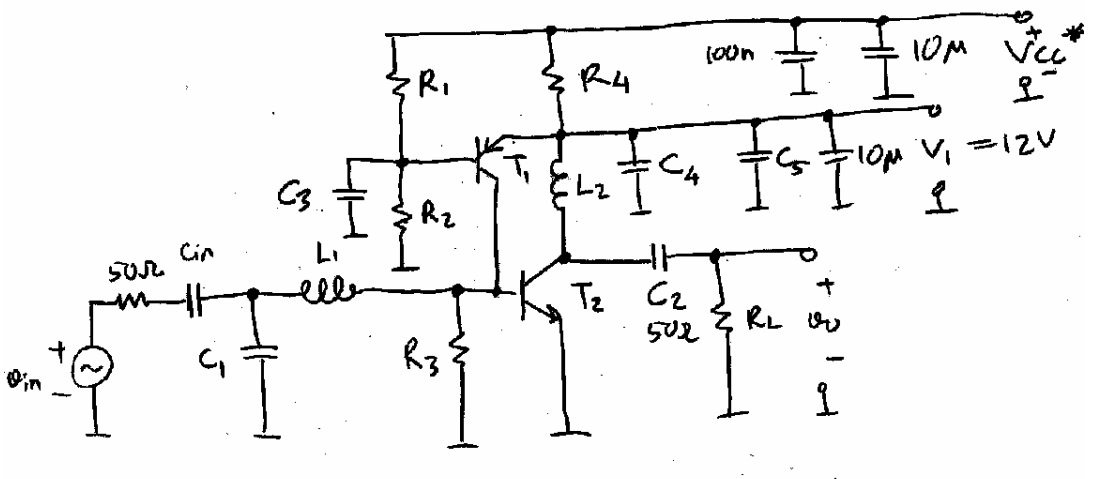
EEE411/EEE511 LAB # 6

Power Amplifiers

Preliminary work:

Design a class-A power amplifier which delivers 0.5W into 50 Ohm load for 28-29.7 MHz band at maximum efficiency using a 12Volts power supply (V1). Note that the BW defines the upper limit of the Q of the circuit. A lower value for Q can be used if practical. Assume that you can achieve $10V_{peak}$ voltage swing on the optimum load resistance (i.e. at the collector of the transistor) and note that 50 Ohm resistor may not be the optimum load.

1. Calculate the optimum load resistance and design the matching network for the output (L_2 and C_2).
2. The input impedance of T1 is equal to 7.5+j 5.55. Calculate the input matching network (L_1 and C_1) to make the input impedance 50 Ohms.
3. T2 is used to keep the collector current of T1 at a fixed bias current. Calculate the collector current of T2 and explain how this circuit works (Please note that using emitter ballast resistor bypassed by a capacitor is not practical for power amplifier since it modifies the input impedance of the amplifier in an uncontrolled manner. That is why a more complicated circuit which controls the bias current by measuring the collector current is chosen). Choose the DC supply voltage such that the collector-emitter voltage of T1 is equal to 12 V. Calculate the power supply drain and efficiency of the amplifier.
4. Choose Cin, C3, C4, C5 to operate the amplifier properly.
5. Check the small signal operation and bias currents of the transistors by SPICE simulation.
6. Plot the bandwidth of amplifier between 1-30MHz by using SPICE simulation.



At the circuit above; R1=150Ω, R2=1k Ω, R3=1.5k Ω, R4=10 Ω, RL=50 Ω, T_1 is BC308 and T_2 is QN3866.

Lab work:

1. Assemble the circuit on a PCB.
2. Measure the D.C. bias of the transistor first. The emitter current of T_1 must be approximately 100mA and the collector-emitter voltage of T_1 must be approximately 12 Volts.
3. Adjust the amplitude of the signal generator to get 0.5 W on the load. It is not allowed to exceed 2Vp-p at the base-emitter junction of T_1 (Check and note DC current by measuring emitter voltage). Proceed to the next step even if you could not get the desired power output.
4. Measure the input impedance of the amplifier using a network analyzer in the frequency band of interest. If it deviates from 50Ω to the extent which limits the power output, then adjust the input impedance to approximately to 50Ω by changing L_1 and C_1, so that the amplifier is driven properly at the input.
5. At the previous step if you still cannot get 0.5 W power output increase the D.C. current of the transistor to get 0.5 W output by changing the base bias of T2.
6. If you still cannot 0.5W output check the output matching by measuring the input impedance of the output matching network by separating it from the collector of the transistor T_2 and please use a DC blocking capacitor in order to protect the input of the network analyzer.
7. Measure the bandwidth of amplifier using LabView
8. Measure DC power drawn (at midband) and calculate the efficiency and Power Added Efficiency.
9. Comment on why the DC current of the transistor changes with the input drive at the previous steps.

Discussion:

Compare your experimental results with your estimations and spice simulations.
Comment on the results.
SPICE Model:

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.MODEL Q2N3866 NPN ( IS = 9.798605E-15 BF = 145.568899 NF = 1.007933 +VAF =
64.3030691 IKF = 0.3661244 ISE = 1.806705E-14 NE = 1.6207001 +BR = 10.471 NR =
1.0003673 VAR = 8.322 IKR = 0.1449443 ISC = 3.326752E-15
+NC = 1.1076801 RB = 15.986 IRB = 2.530217E-3 RBM = 0.01 RE = 0.02604
+RC = 1.0359 CJE = 9.055532E-12 VJE = 0.6761546 MJE = 0.2754969
+TF = 1.25476E-10 XTF = 13.0616413 VTF = 0.4699 ITF = 0.2828
+PTF = 18.9645325 CJC = 7.054363E-12 VJC = 0.5769848 MJC = 0.3139067
+XCJC = 1 TR = 5.698362E-8 CJS = 0 VJS = .75 MJS = 0 XTB = 1.831
+EG = 1.11 XTI = 5.0205 KF = 0 AF = 1 FC = 0.9 )
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