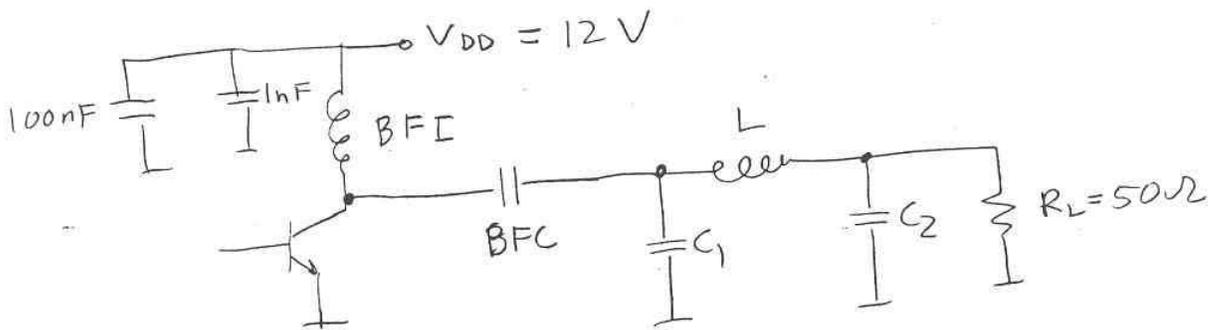


16 Jan, 2004, 15.30

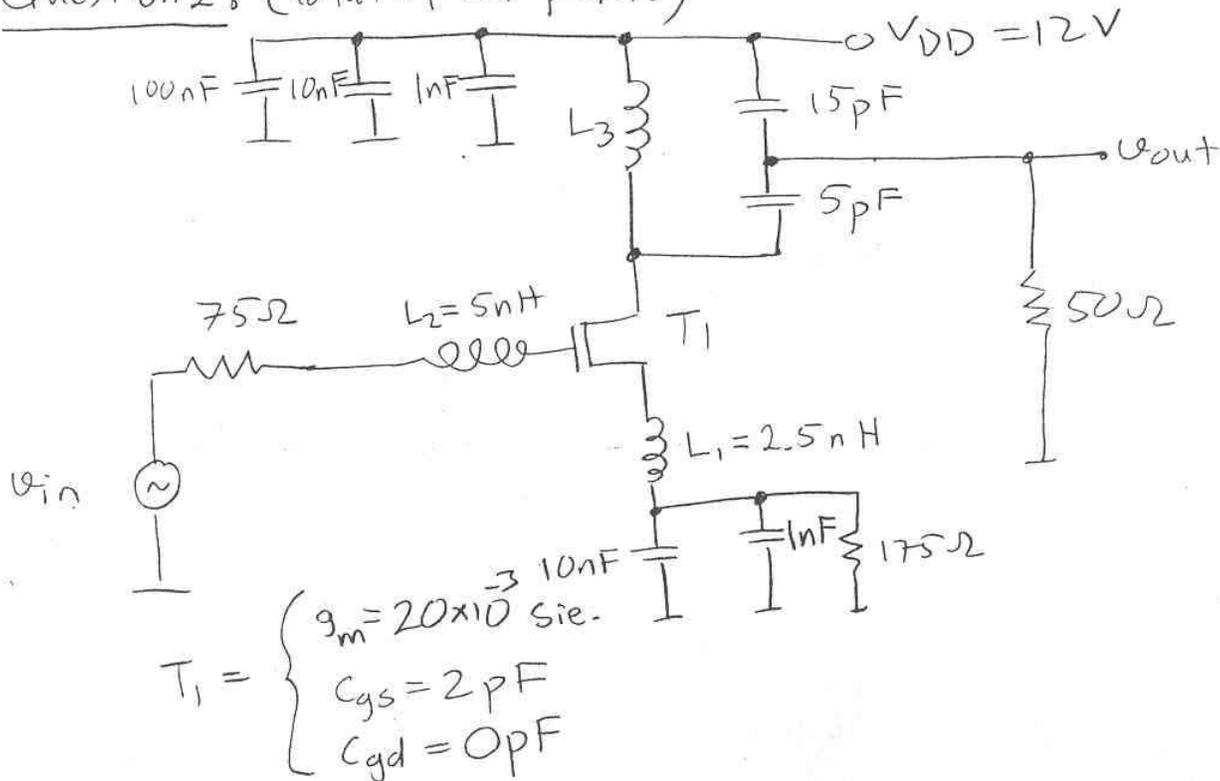
Question 1: (20 points)

The class C amplifier shown above is designed to deliver 48 Watts into  $50\Omega$  load with maximum efficiency. The operating frequency and the bandwidth of the amplifier are 15.915 MHz and 1.5915 MHz respectively. Find the component values of  $L$ ,  $C_1$  and  $C_2$ . Assume an ideal transistor and lossless passive components.

a-) 8 puan  $\rightarrow R_{opt}$   
 12 puan  $\rightarrow$  matching

16 Jan, 2004 15-30

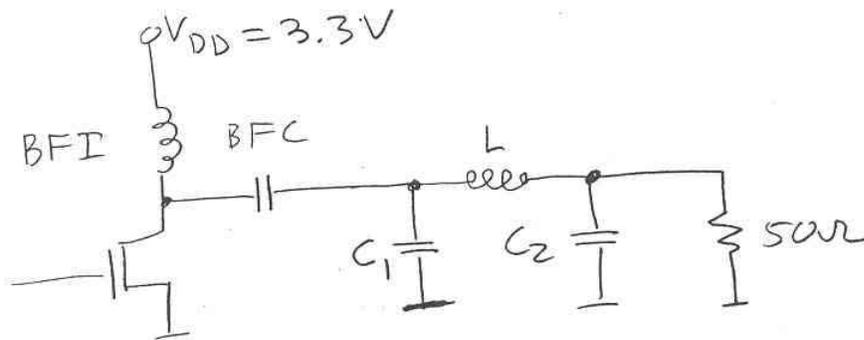
Question 2: (Total of 24 points)



An amplifier as shown above was constructed using a transistor with parameters shown at the figure. Assume that the D.C. bias conditions are satisfied.

- a-) (8) Find the resonance frequency of the amplifier.
- b-) (8) Find the value of  $L_3$  which maximizes the gain at the resonant frequency.
- c-) (8) Find the gain at the resonant frequency for the value of  $L_3$  calculated at step (b), (Gain is defined by  $G = \frac{V_o}{V_{in}}$  as marked in the figure).

16 Jan, 2004, 15:30

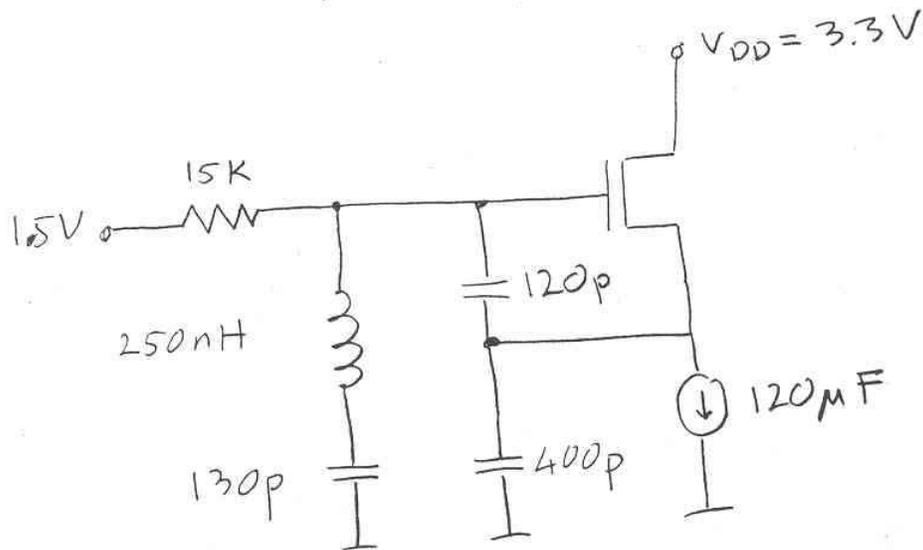
Question 3: (Total of 16 points)

A class A power amplifier has been designed to deliver 100mW power output into 50Ω load at 2.45 GHz for the BW of 90MHz for wireless applications to operate at maximum efficiency at 100mW output. Assume all the passive components are lossless and the transistor is ideal.

a-)(8) Find the optimum impedance which must be seen by the transistor.

b-)(8) This type of amplifier is used to amplify signals which can be modelled by two simultaneous sinusoids of equal amplitude typically twice the chip-rate apart in the frequency domain. The power amplifiers must be extremely linear. Find the maximum power output which can be obtained from the amplifier designed at (a) if driven by such a signal as specified above.

16 Jan, 2004, 15-30

Question 4: (Total of 20 points)

For the circuit given above:

- a-)(6) Calculate the oscillation frequency
- b-)(7) Calculate the amplitude of the oscillation at the gate.
- c-)(7) Find the voltage on the inductor.

Note: Assume an ideal transistor with large enough  $g_m$  to start oscillation.

16 Jan, 2004 15-30

Question 5 (Total of 20 points)

A PLL frequency synthesizer is needed for bluetooth applications. The operation frequency band is 2.4-2.5 GHz. Channel spacing is 100 kHz. The first frequency starts at 2.4 GHz. The frequency is so high that counters can not function without a prescaler. A dual modulus prescaler dividing to 32/33 must be used. Reference frequency must be 100 kHz.

- a-) (5 Points) Draw the block diagram of the frequency synthesizer; name all the blocks to show their functions and label the frequencies.
- b-) (5 Points) Find what values must be loaded to the counters to synthesize 2.455 GHz.
- c-) (5) A new requirement comes up with the same specifications except that the first frequency must be 2.40004 GHz again with the same channel spacing. Modify your block diagram to accommodate for the change.
- d-) (5) Find what values must be loaded to the counters for the synthesizer at step (c) for synthesizing the frequency 2.45524 GHz.