MOS: Metal-oxide-semiconductor

Dominant MOS logic family based on CMOS (comlementary MOS).
There are other MOS logic families: NMOS, PMOS, domino, pass-transistor, etc, etc

Real-life (death or life)/(promotion or door) questions:

Why is MOS faster than BJT? Is MOS faster than BJT?
Why can BJT drive interchip lines better?
Will MOS be forever?
Why do we still need new alternatives?
    (SOI, SiGe, BiCMOS, strained Si/SiGe BiCMOS, GaAs?, nanotube)
If somebody asks you to design/implement some logic function who do you call?
    (ALS-TTL or CMOS or BiCMOS)

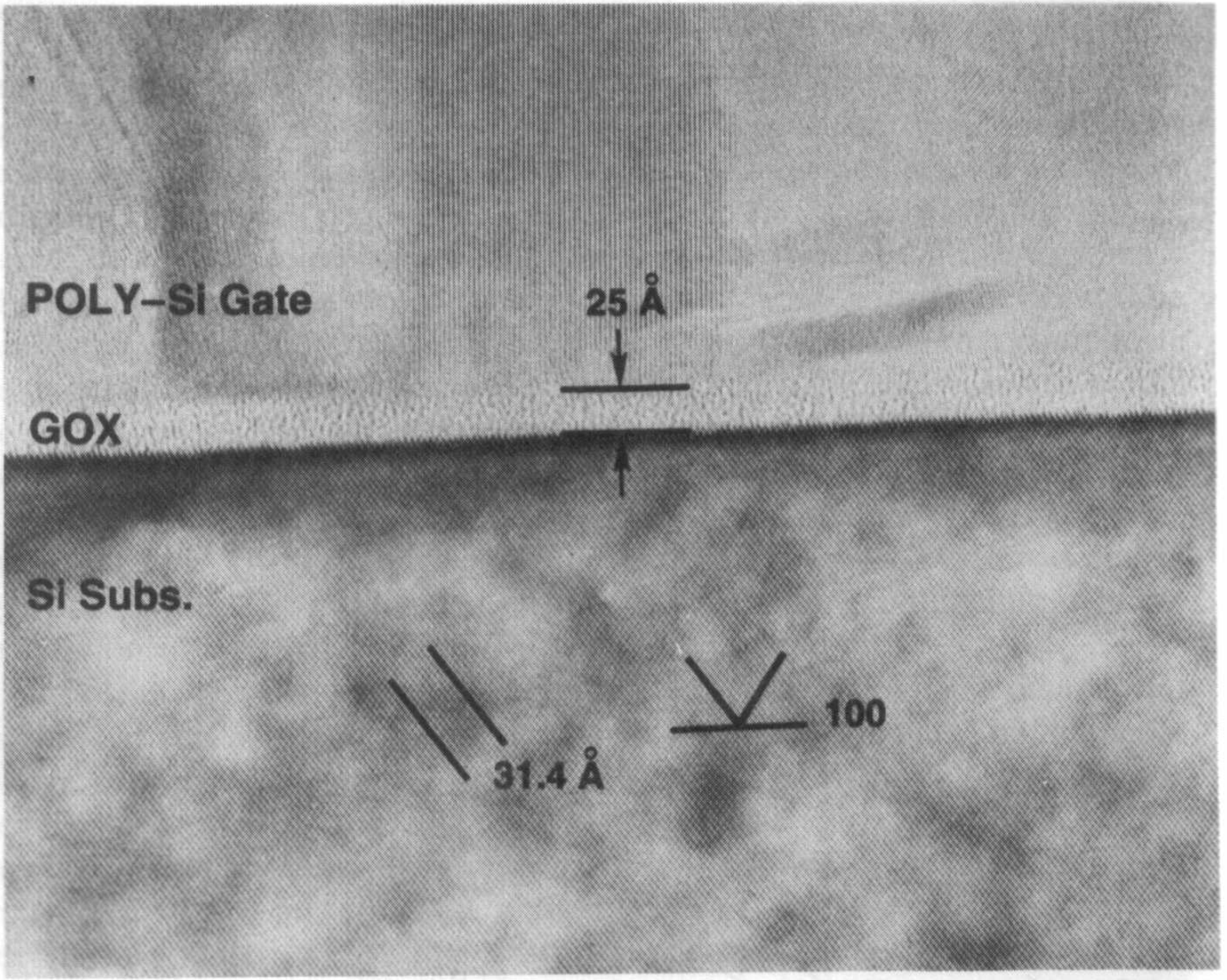


Fig. 12 TEM cross-section of a 2.5 nm (25 Å) gate oxide. The lattice spacing of the silicon substrate is used to accurately determine the oxide thickness. (After Liu et al., Ref. 15. Copyright © 1996 IEEE.)

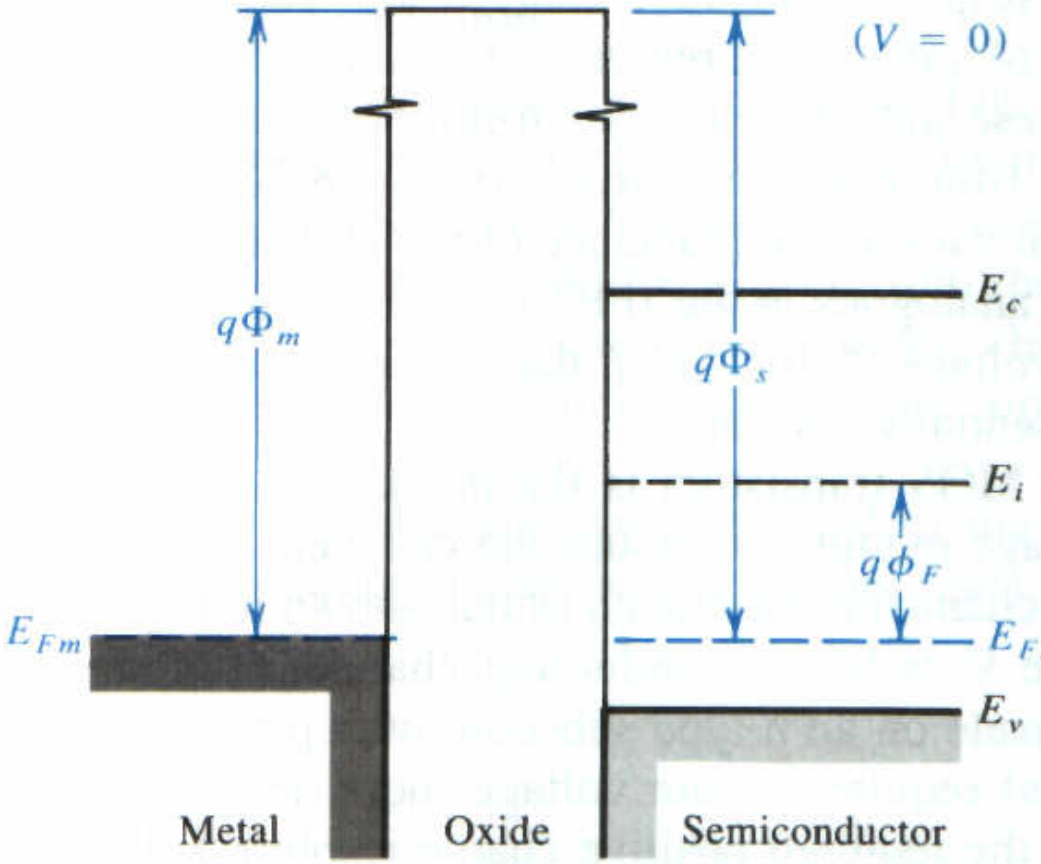
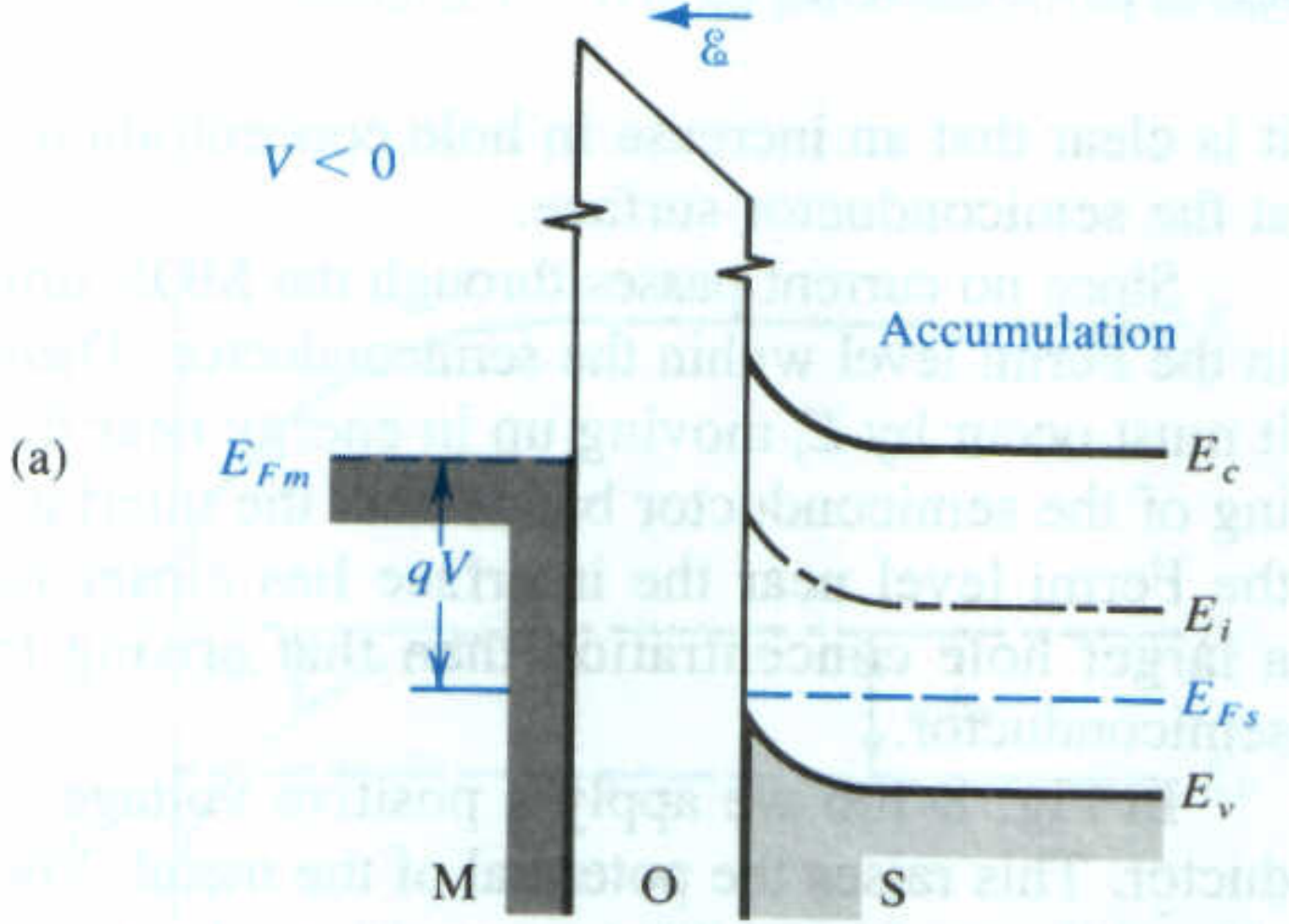
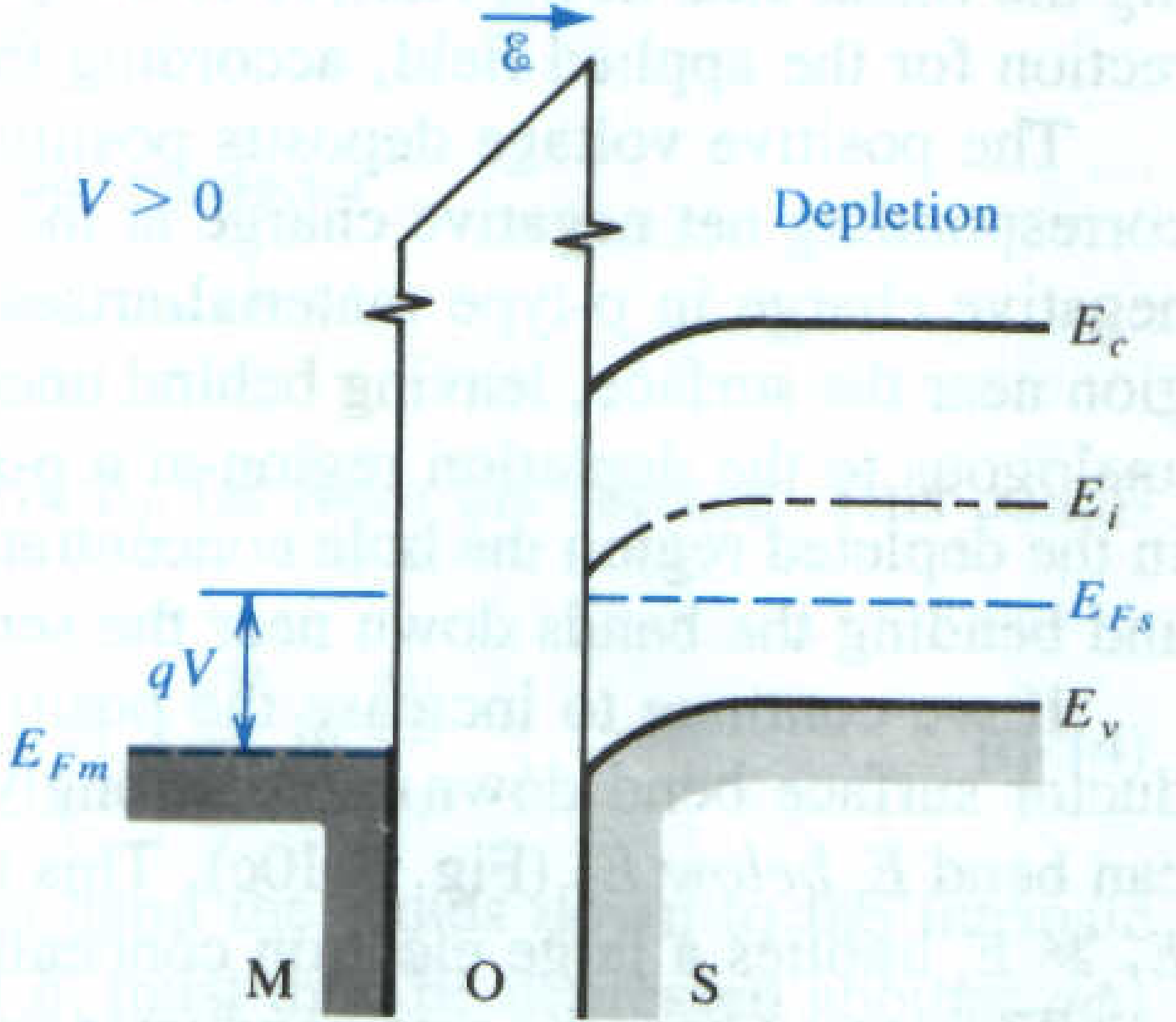


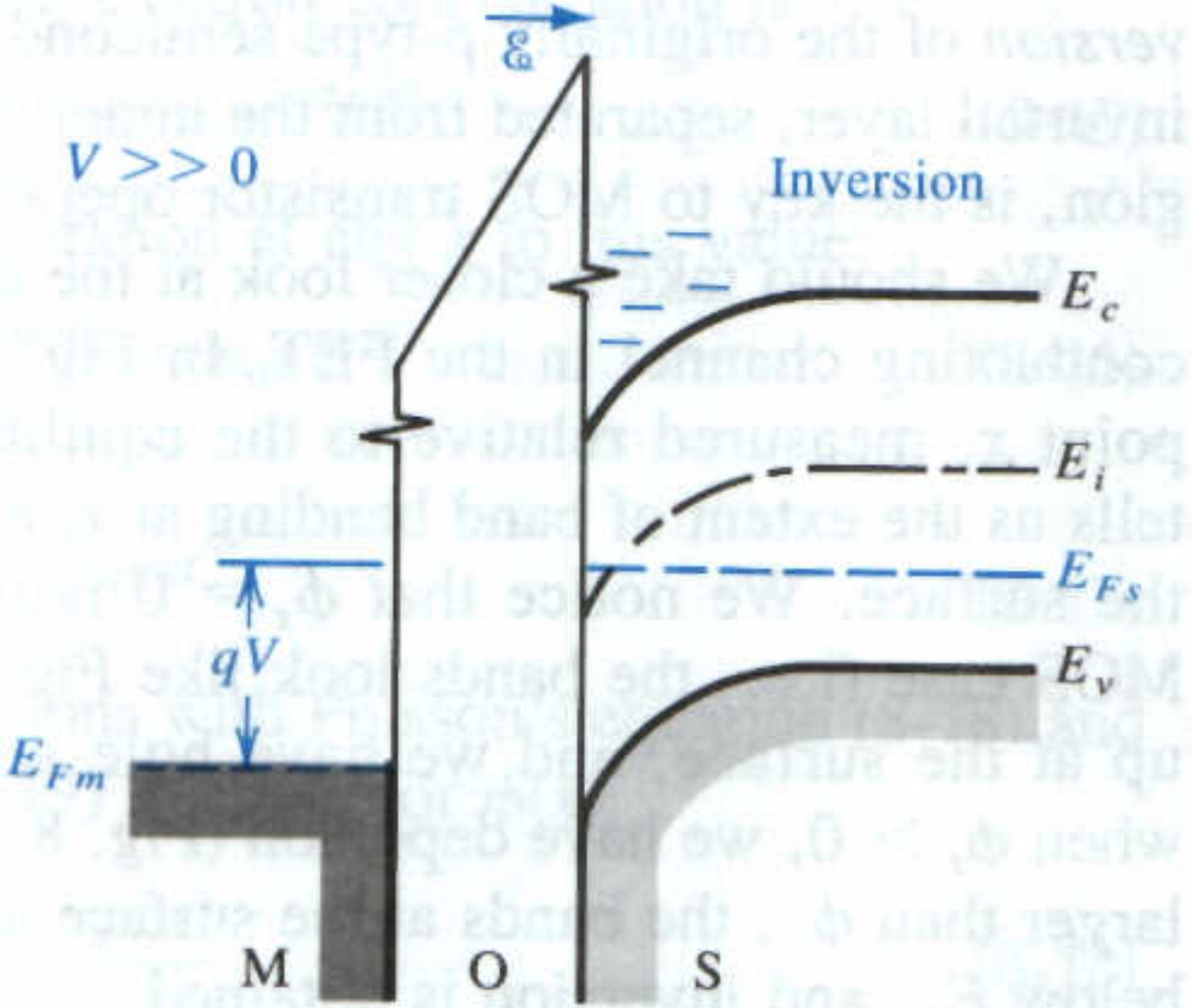
Figure 8-9
Band diagram for the ideal MOS structure at equilibrium.


(a)
$V < 0$
$\mathcal{E}_g$
Accumulation
E_{Fm}
qV
E_c
E_i
E_{Fs}
E_v
M
O
S

(b)



(c)



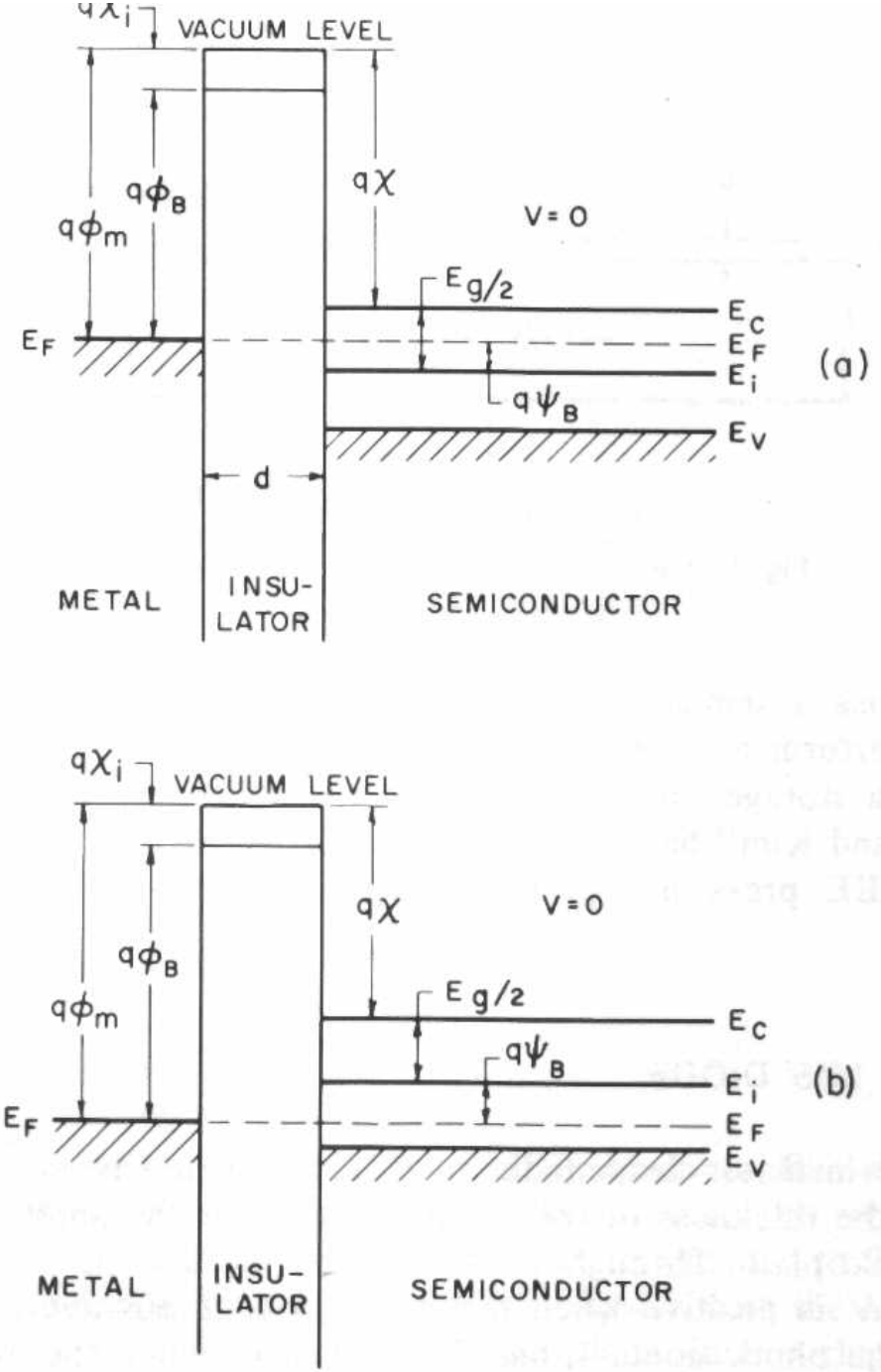


Fig. 2 Energy-band diagrams of ideal MIS diodes at $V = 0$. (*a*) *n*-type semiconductor (*b*) *p*-type semiconductor.

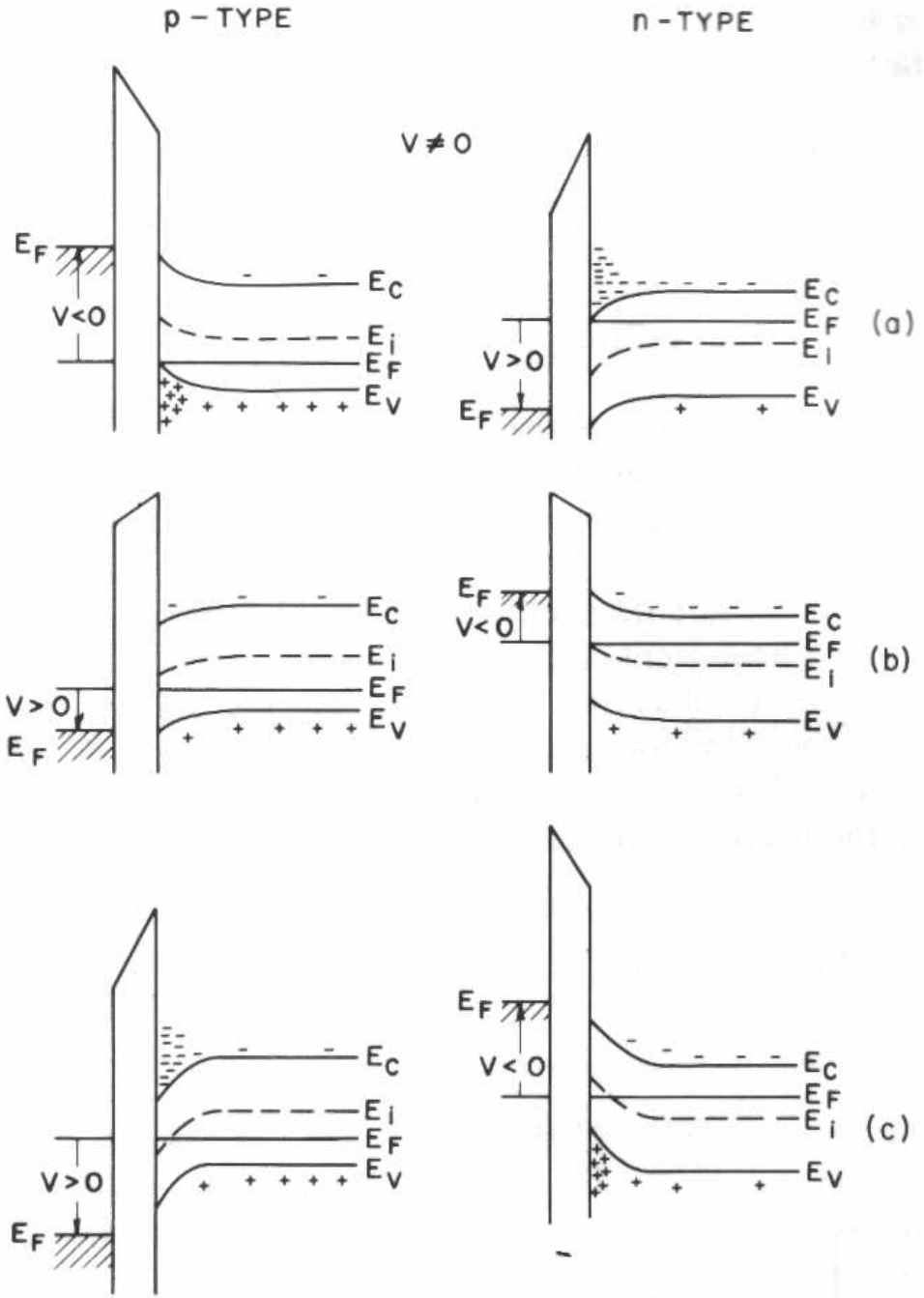


Fig. 3 Energy-band diagrams for ideal MIS diodes when $V \neq 0$, for the following cases: (*a*) accumulation; (*b*) depletion; (*c*) inversion.

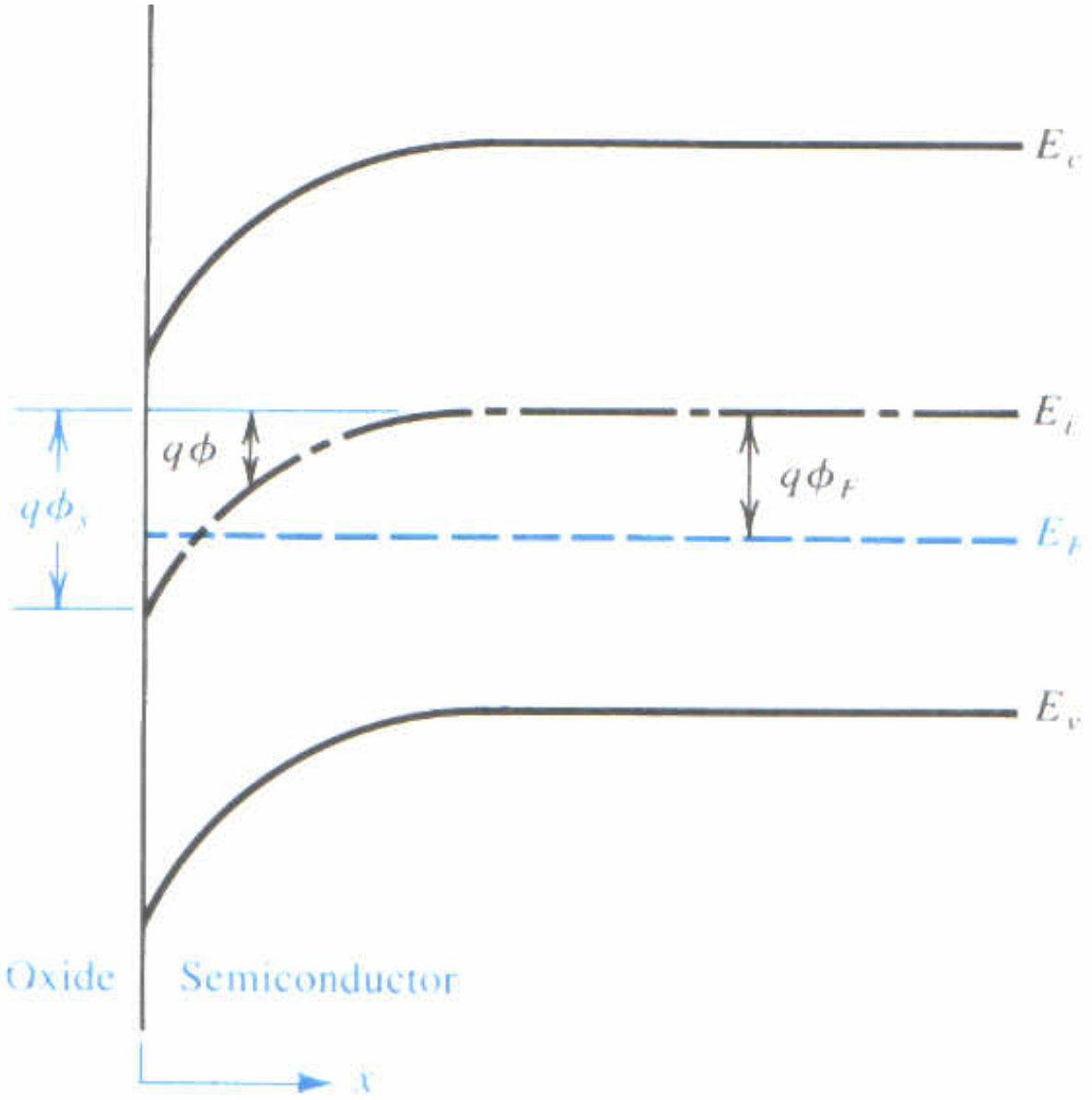


Figure 8-11
Bending of the semiconductor bands at the onset of strong inversion: the surface potential ϕ_s is twice the value of ϕ_F in the neutral p material.

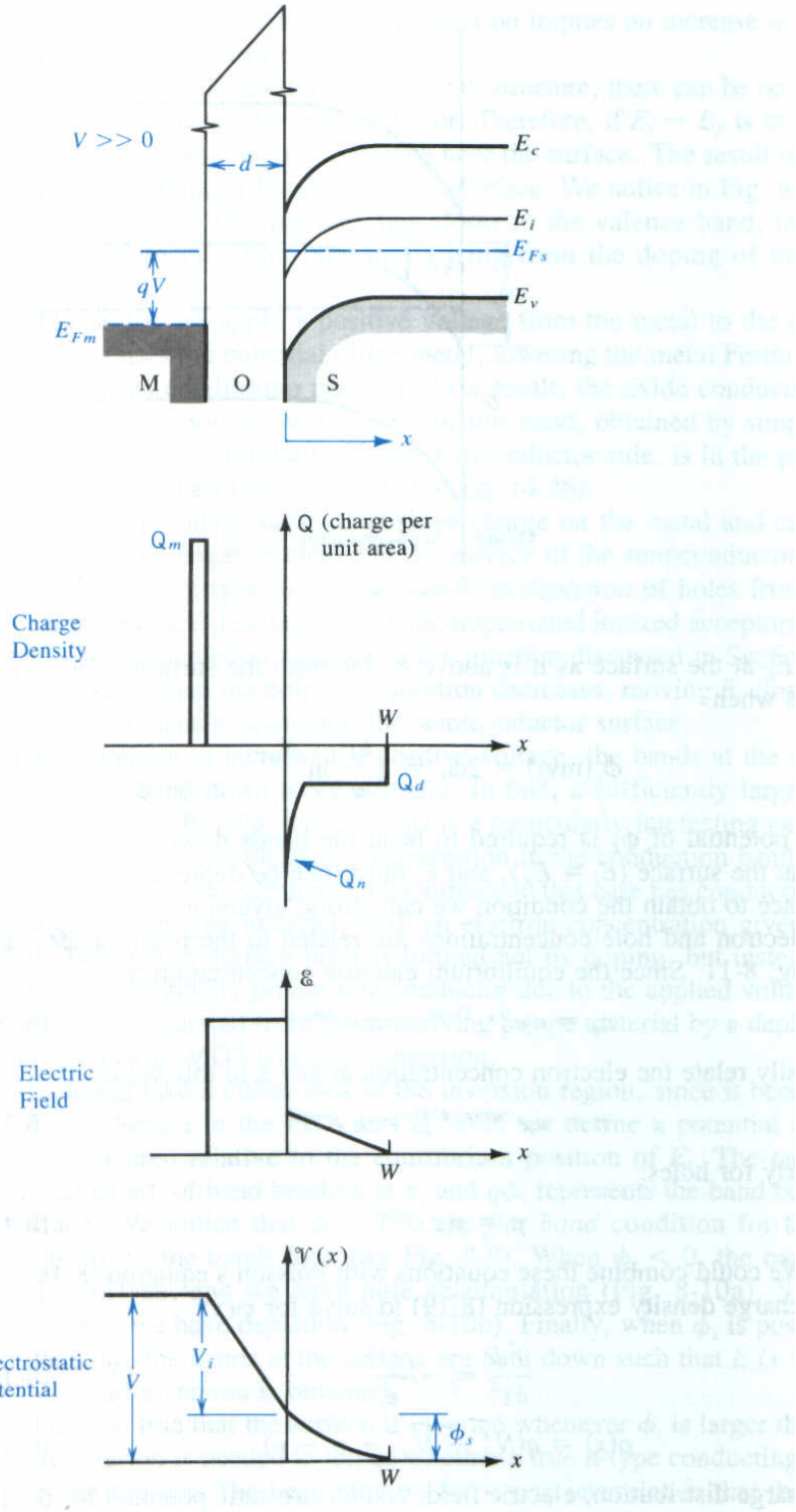


Figure 8-12 Approximate distributions of charge, electric field, and electrostatic potential in the ideal MOS capacitor in inversion. The relative width of the inverted region is exaggerated for illustrative purposes, but is neglected in the field and potential diagrams.

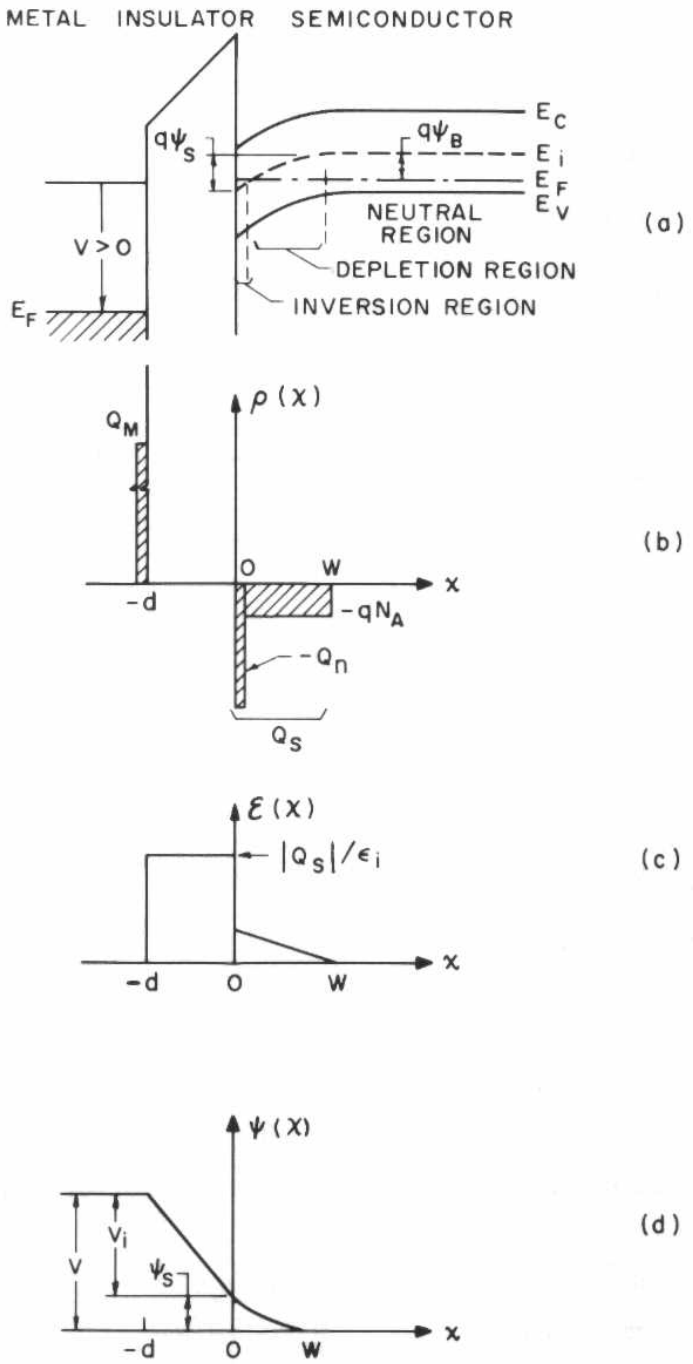
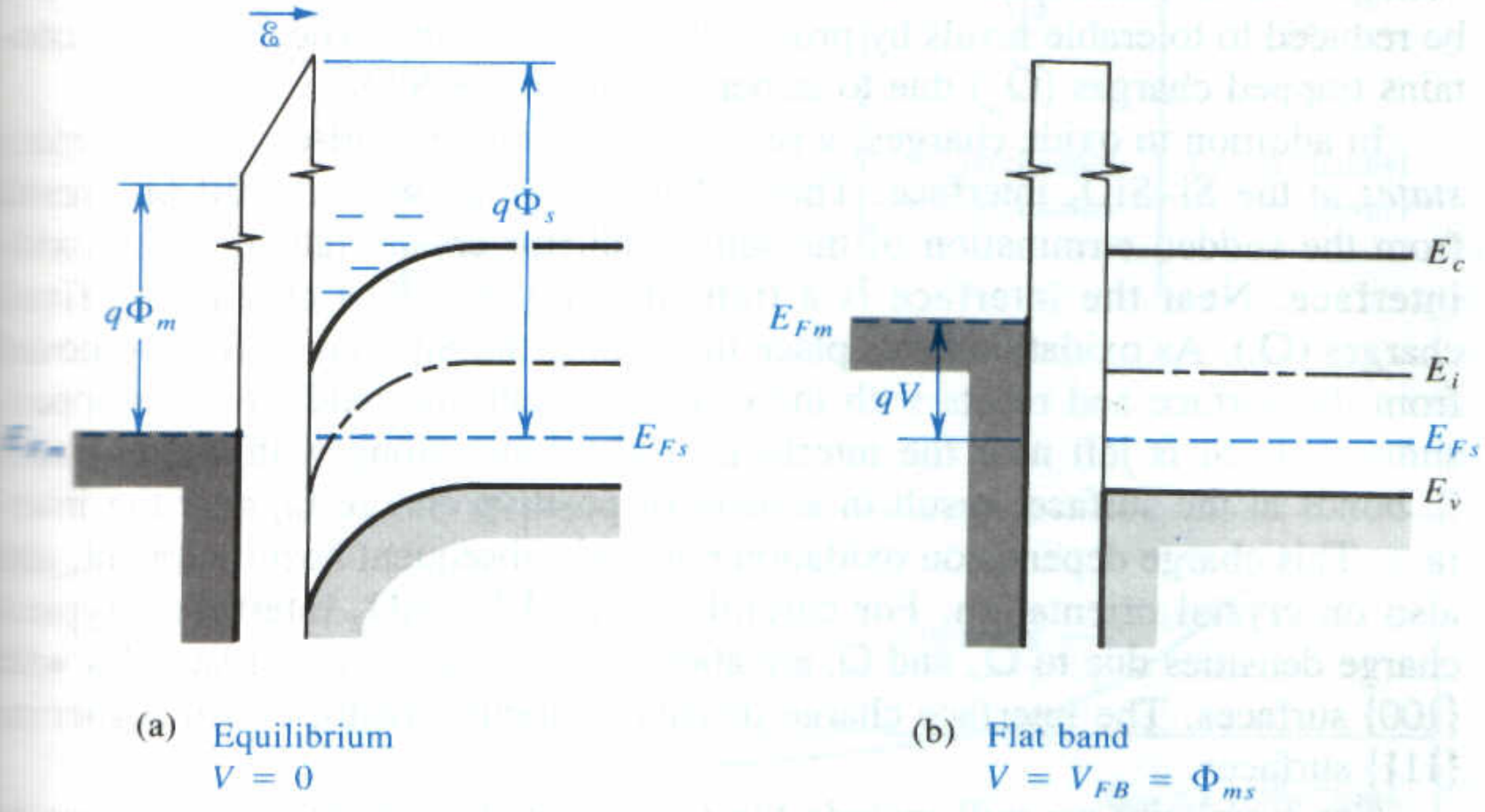


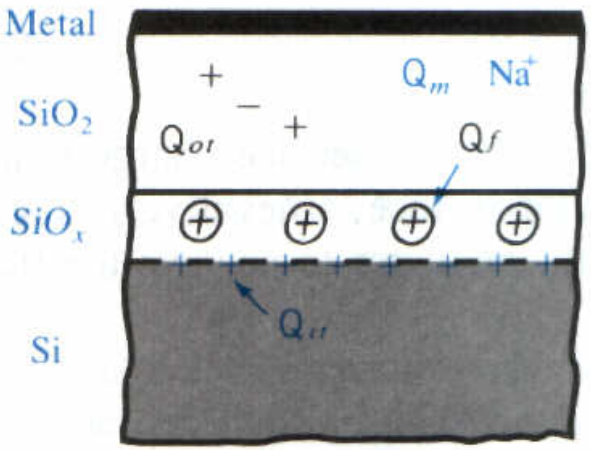
Fig. 6 (*a*) Band diagram of an ideal MIS diode. (*b*) Charge distribution under inversio condition. (*c*) Electric field distribution. (*d*) Potential distribution.



(a) Equilibrium
$V = 0$

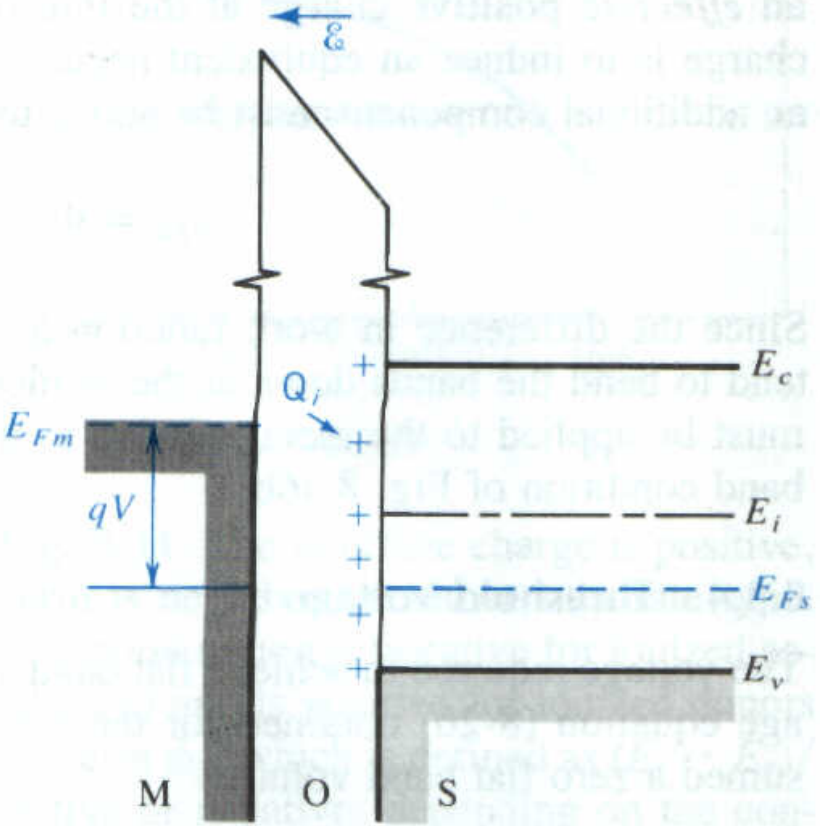
(b) Flat band
$V = V_{FB} = \Phi_{ms}$

Figure 8-15
Effect of a negative work function difference ($\Phi_{ms} < 0$): (a) band bending and formation of negative charge at the semiconductor surface; (b) achievement of the flat band condition by application of a negative voltage.



Q_m Mobile ionic charge
Q_{ot} Oxide trapped charge
Q_f Oxide fixed charge
Q_{it} Interface trap charge

(a)



$$V = V_{FB} = -\frac{Q_i}{C_i}$$

(b)

Figure 8-16
Effects of charges in the oxide and at the interface: (a) definitions of charge densities (C/cm^2) due to various sources; (b) representing these charges as an equivalent sheet of positive charge Q_i at the oxide–semiconductor interface. This positive charge induces an equivalent negative charge in the semiconductor, which requires a negative gate voltage to achieve the flat band condition.

(a)

$V_T =$	Φ_{ms}	$-\frac{Q_i}{C_i}$	$-\frac{Q_d}{C_i}$	$+ 2\phi_F$
	(−)	(−)	(+) n channel (−) p channel	(+) n channel (−) p channel

Figure 8-17
Influence of materials parameters on threshold voltage: (a) the threshold voltage equation indicating signs of the various contributions; (b) variation of V_T with substrate doping for

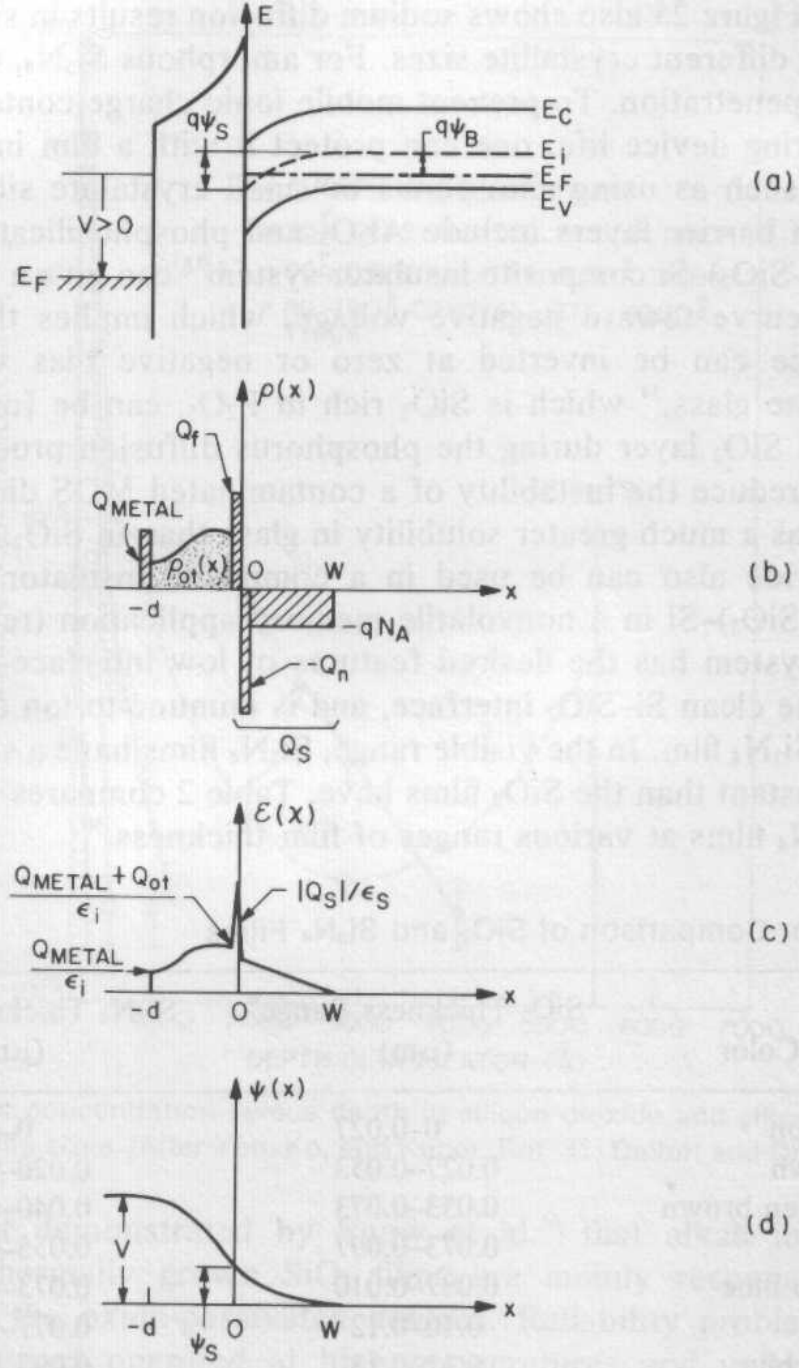


Fig. 26 An MIS diode with fixed oxide charge and oxide trapped charge. (a) Band diagram. (*b*) Charge distribution. (*c*) Field. (*d*) Potential.

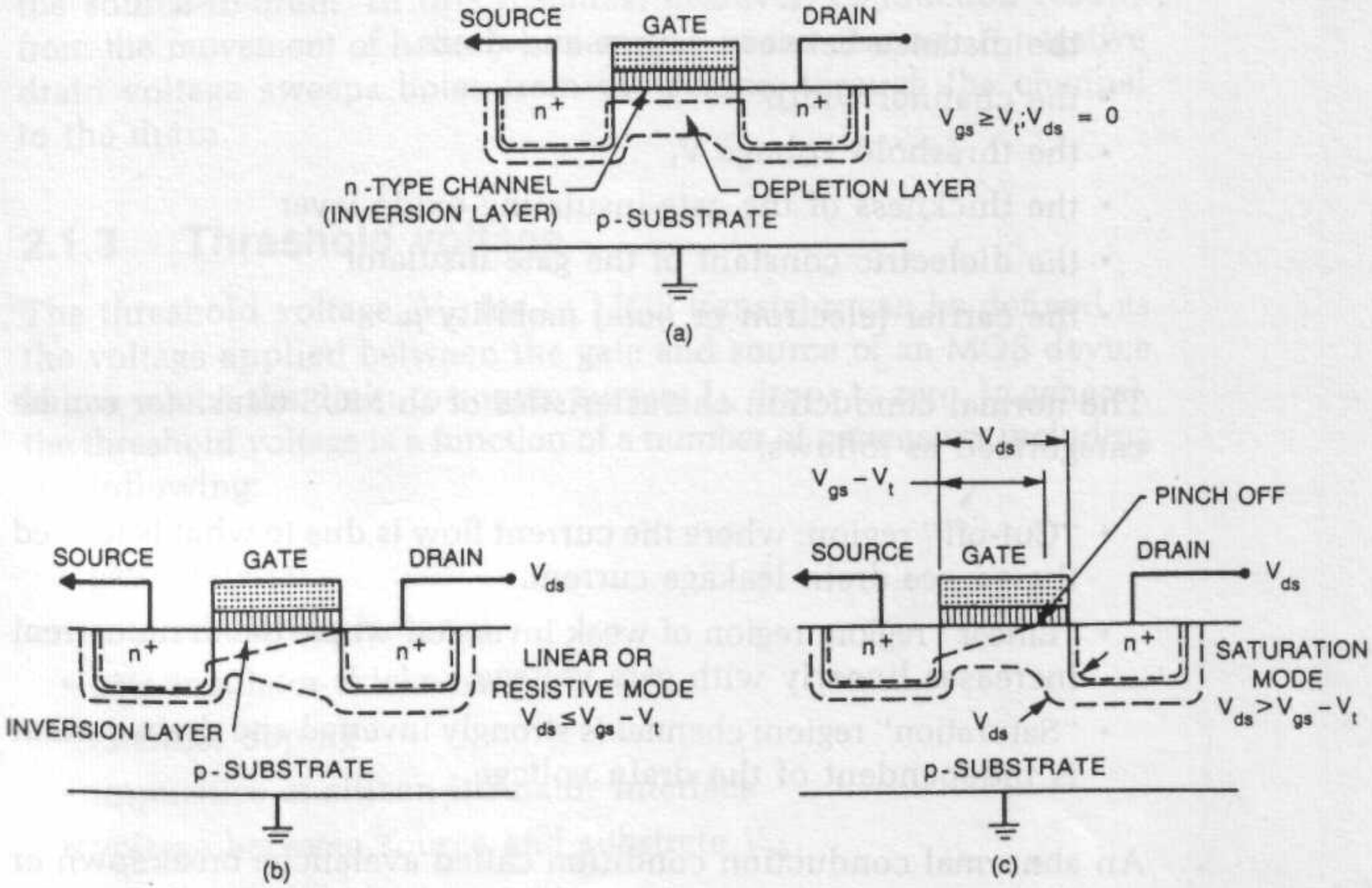
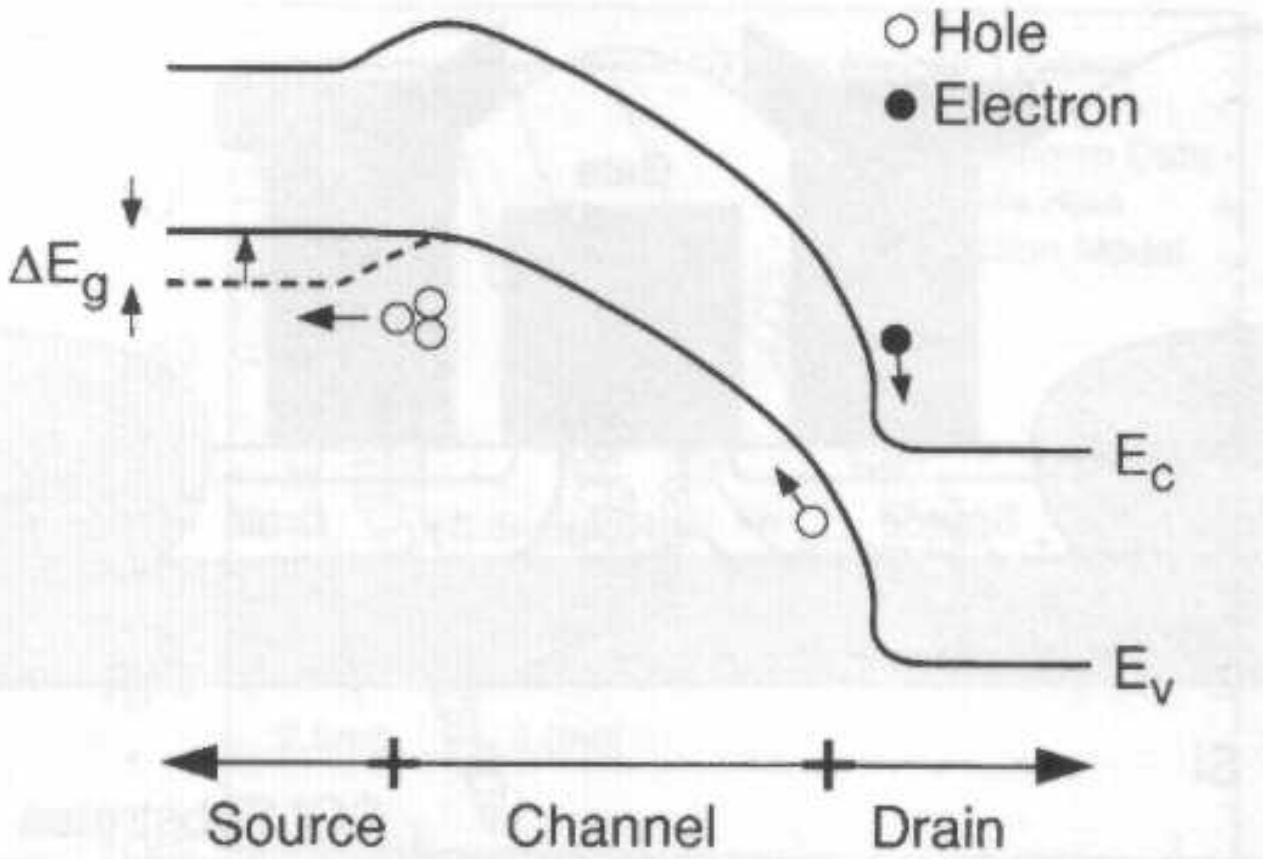


FIGURE 2.5. nMOS device behavior under the influence of different terminal voltages


Hole
Electron
ΔE_g
E_c
E_v
Source
Channel
Drain

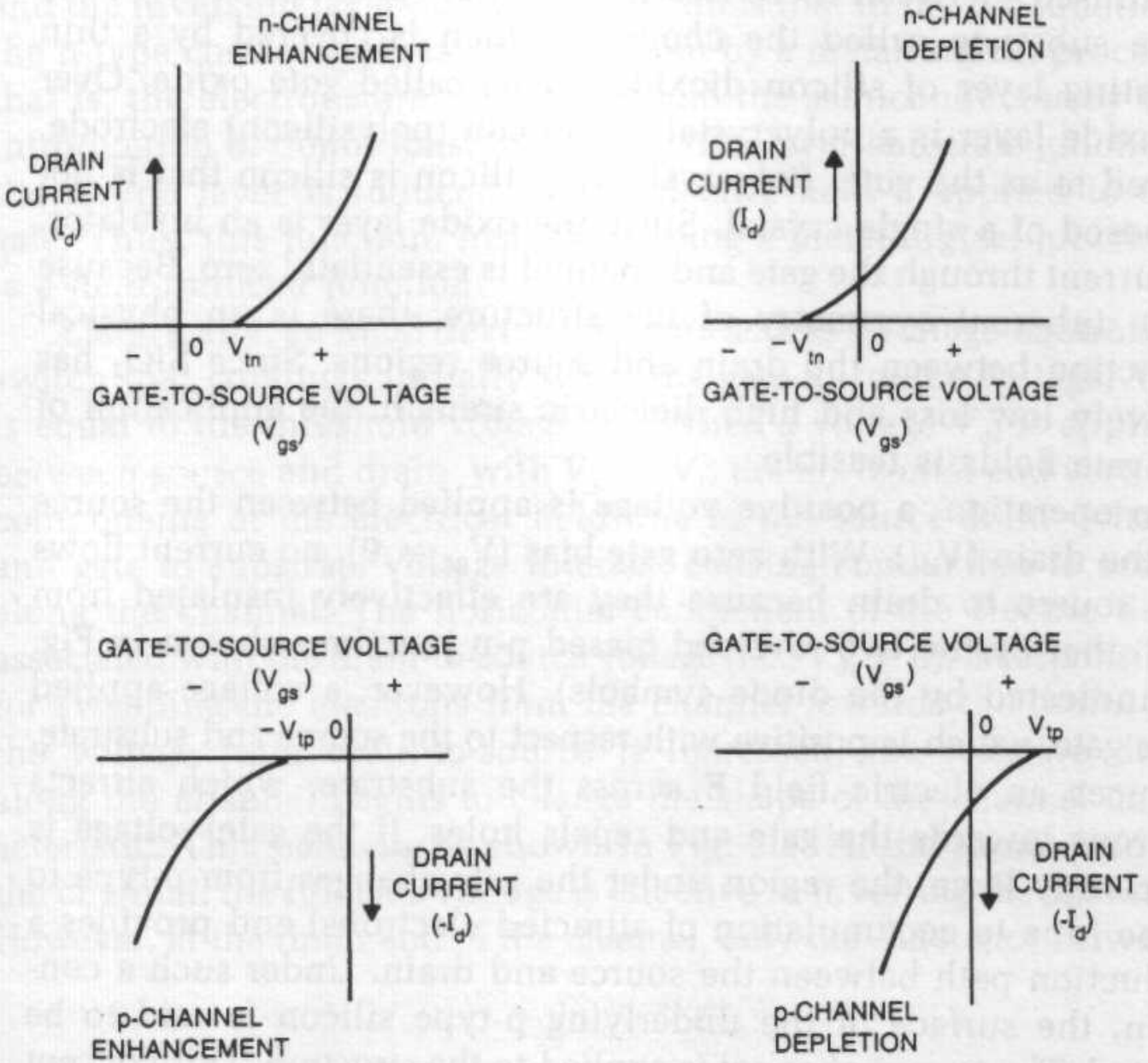


FIGURE 2.2. Conduction characteristics for enhancement and depletion mode transistors (assuming fixed V_{ds})

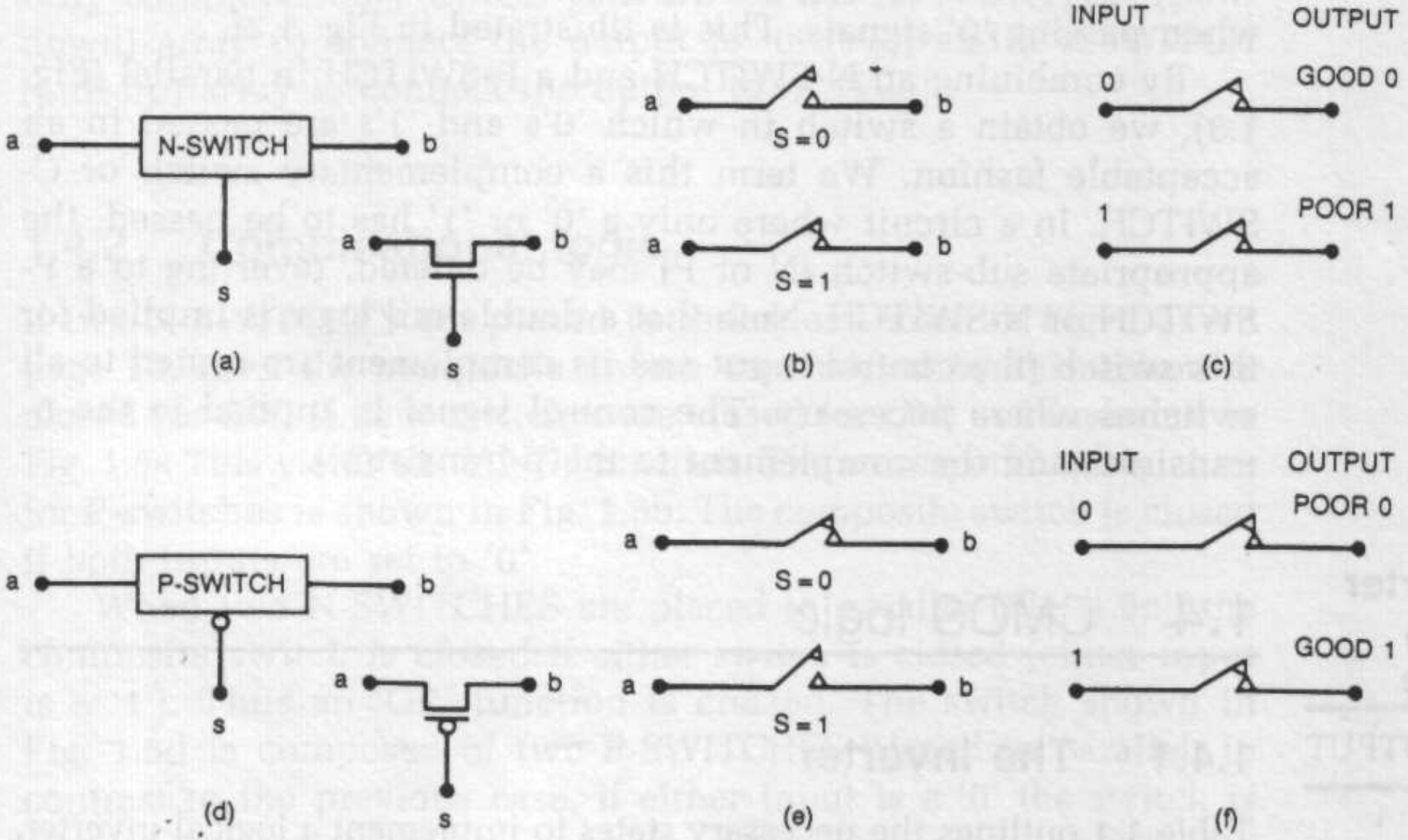


FIGURE 1.2. MOS transistors viewed as switches