EEE 314 LAB #4 MANUAL

The aim of this lab is to familiarize ourselves with the fundamental working mechanisms of MOS structures. The objective is to be able to extract the MOS parameters after certain measurements and also to examine the transition times for CMOS inverters.

PRELAB

Part1

NMOS	PMOS
$V_{thn} = 0.7V$	$V_{thp} = -0.8V$
$k_n = 0.6mA/V^2$	$k_p = 0.5mA/V^2$
$\gamma_n = 0.5\ V^{1/2}$	$\gamma_p = 0.2\ V^{1/2}$
$\lambda_n = 0.1\ V^{-1}$	$\lambda_p = 0.2\ V^{-1}$

Table 1 MOS parameters for Part1

* You may take $2\Phi_{Fn}=2\Phi_{Fp}=0.6$ Volts

a) Use the parameters given in Table 1 as inputs for a MATLAB program that plots Ids as a function of Vgs for circuits given in Figure 1. |Vgs| might vary in between 0 and 1.5 Volts. Attach your code. Your graphs will look like the following (Figure2). Be careful with the signs and clearly indicate the NMOS and PMOS plots. Make all necessary assumptions. Ignore the voltage drop over the resistance (RD) at the drain sides.

b) Using the given parameters above, write a MATLAB program to plot Ids vs Vds for the circuits given in Figure3. Vapplied might vary in between 0 and Vdd = 5Volts. On the same figure plot for different Vgs voltages. |Vgs| might take values in between 1Volt up to 3Volts. Do not forget to handle the body effect. For another |Vsb| you may choose, comment about the influence of the body effect on Ids vs Vds curves. Attach your code. Your graphs will look like the following (Figure4), clearly indicate each Vgs voltage that you have used. Make all necessary assumptions. Ignore the voltage drop over the resistance (RD) at the drain sides. You may artificially add the effect of channel length modulation in linear region as well to avoid the discontinuity at the transition.

Part2

a) The student has an NMOS device. He builds the same circuit given in Figure3 (circuit for the NMOS transistor) to estimate the channel length modulation (λ_n) of his NMOS transistor. He assures that his transistor is in saturation (Vsb=0.5 Volts, and Vgs=2 Volts) and measures the following values for Vds vs Id (Table 2). Extract the channel length modulation.

b) Now, he builds the same circuit given in Figure1 (circuit for the NMOS transistor) to estimate the threshold voltage (Vth) and Kn. For the same circuit (RD = 50 Ohms, Vdd = 5Volts), he measures Ids for different values of Vgs and notes them down (Table 3). Using the measured values in Table3, extract Vth and Kn for this transistor. Make all necessary assumptions.

c) Now the student knows Vth, Kn and λ_n. The only parameter left is the body effect. In order to find it, he builds the same circuit shown Figure3 but now with Vsb=2.5 Volts, and Vgs=2 Volts, for the NMOS transistor and measures Ids vs Vds (Table 4).
Extract the body effect (γ_n). You may take $2\Phi_{Fn}=2\Phi_{Fp}=0.6$ Volts.

Experiment

In this experiment, we are not going to extract the body effect, so you may use the transistors with Vsb=0 for IC 4007 configuration. Work in groups of 2 people. Every group is free to share the power supply voltages of their neighbors'.

1) Come up with an idea to roughly extract λ_n and λ_p of both NMOS and PMOS transistors using Vds vs Ids measurements. Clearly write down the value you have found.

2) Come up with an idea to roughly extract the Vth, Kn and Kp of both NMOS and PMOS transistors using Vgs vs Ids measurements. Clearly write down the value you have found.

3) After having extracted all the parameters, use three different Cload values (560pF, 1.2nF, 10nF), measure the transition times for the inverter configuration in Figure 5. Definitions are given in Figure 6.

Ids, (mA)	Vds, (Volts)
0.4859	1.9757
0.4939	2.1753
0.5020	2.3749
0.5101	2.5745
0.5182	2.7741
0.5263	2.9737
0.5344	3.1733
0.5425	3.3729
0.5506	3.5725

Ids, (mA)	Vds, (Volts)
0.5587	3.7721
0.5668	3.9717
0.5749	4.1713
0.5830	4.3708
0.5911	4.5704
0.5992	4.7700
0.6073	4.9696

Table 2 NMOS Ids vs Vds measured values for Part2a

Ids, (mA)	Vgs, (Volts)
0	0
0	0.1
0	0.2
0	0.3
0	0.4
0	0.5
0	0.6
0	0.7
0.0045	0.8
0.0180	0.9
0.0405	1

Ids, (mA)	Vgs, (Volts)
0.0720	1.1
0.1125	1.2
0.1619	1.3
0.2203	1.4
0.2877	1.5
0.3641	1.6
0.4493	1.7
0.5435	1.8
0.6466	1.9
0.7586	2

Table 3 NMOS Ids vs Vgs measured values for Part2b

Ids, (mA)	Vds, (Volts)
0	0
0.1198	0.2940
0.1920	0.5904
0.2127	0.8894
0.2186	1.1891
0.2244	1.4888
0.2303	1.7885
0.2361	2.0882
0.2420	2.3879

Ids, (mA)	Vds, (Volts)
0.2479	2.6876
0.2537	2.9873
0.2596	3.2870
0.2654	3.5867
0.2713	3.8864
0.2771	4.1861
0.2830	4.4859

Table 4 NMOS Ids vs Vds measured values for Part2c

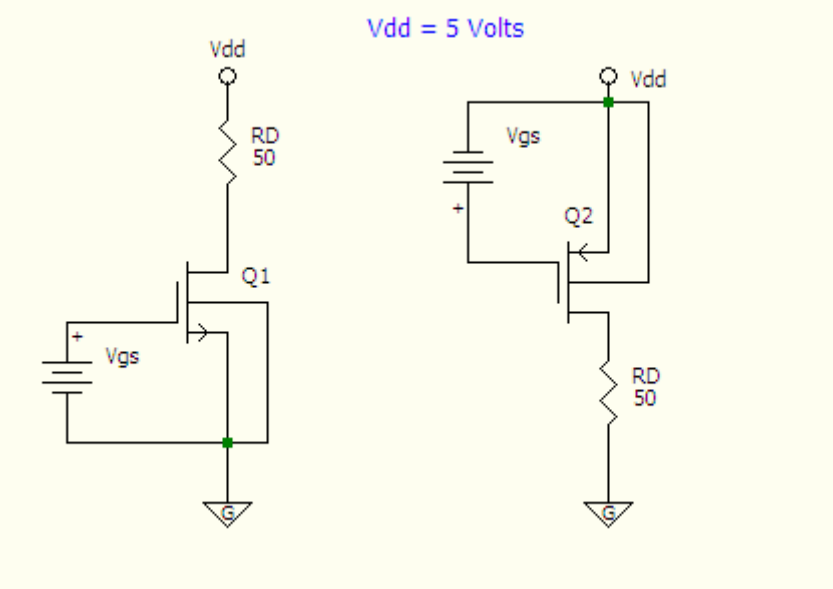

Figure 1 Vgs vs Ids investigation for NMOS and PMOS

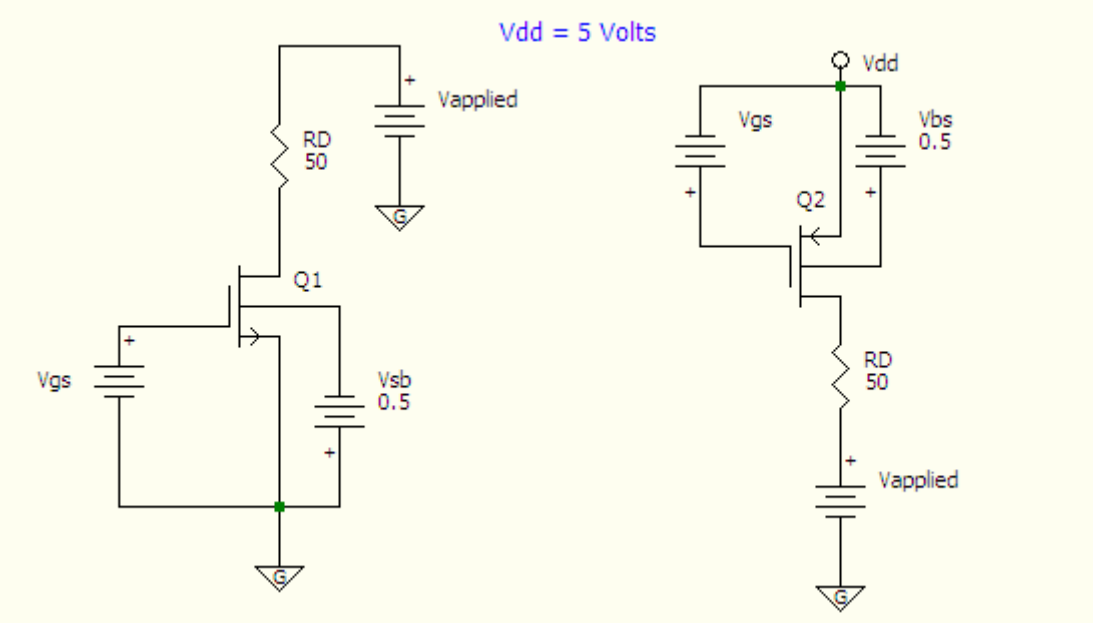

Figure 3 Vds vs Ids investigation for NMOS and PMOS

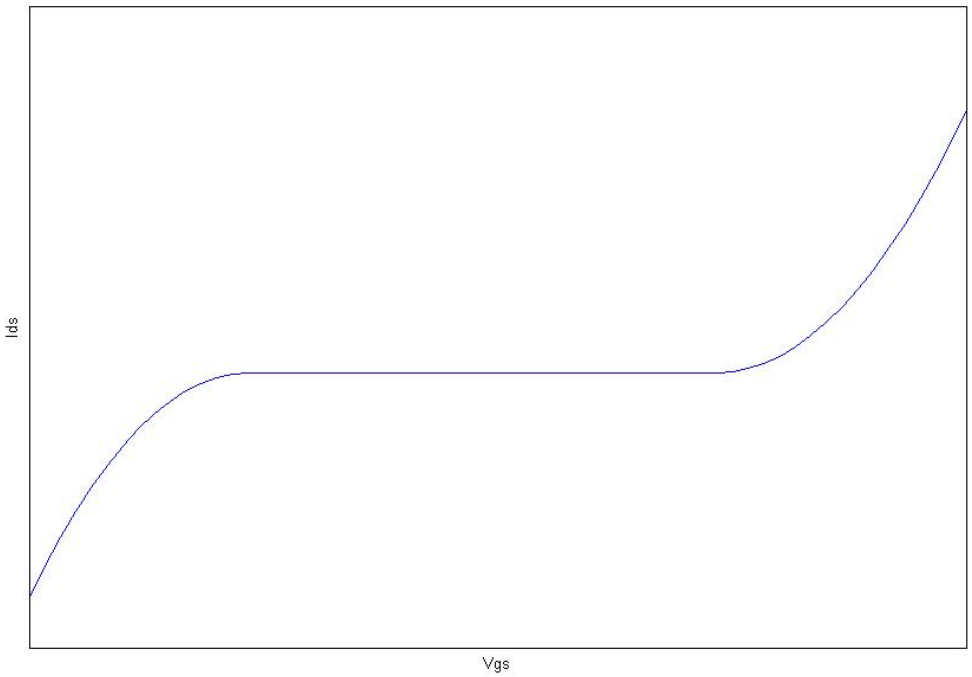

Figure2 An Exemplary Vgs vs Ids curve

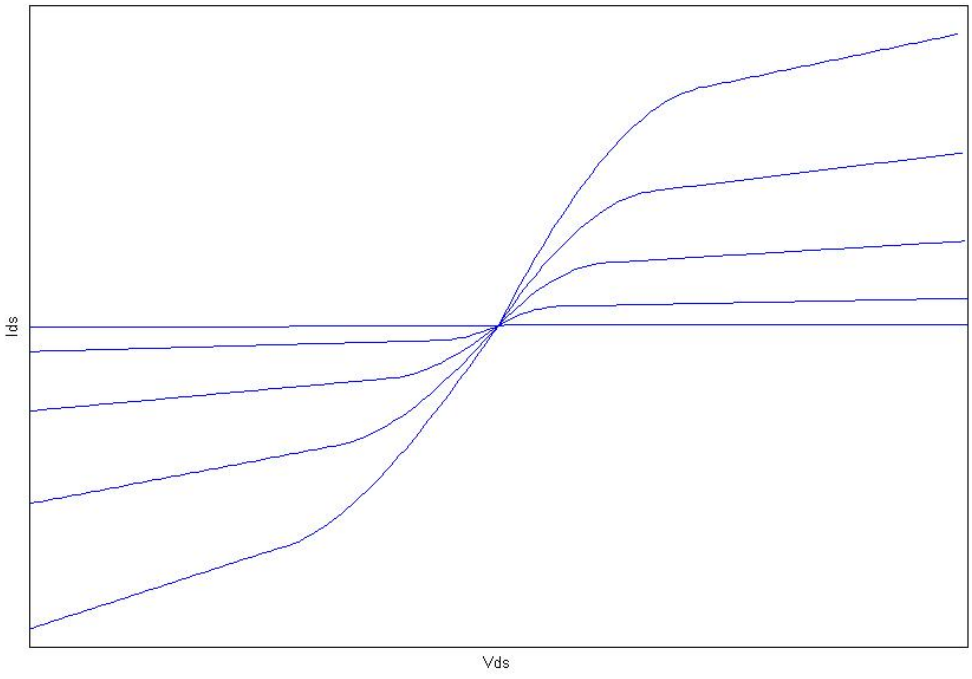

Figure4 An Exemplary Vds vs Ids curve

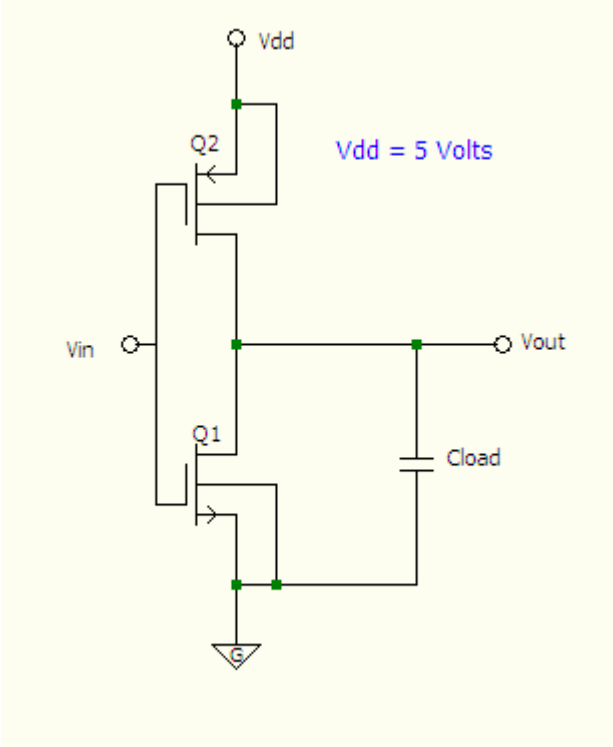

Figure 5 CMOS Inverter with loading capacitance

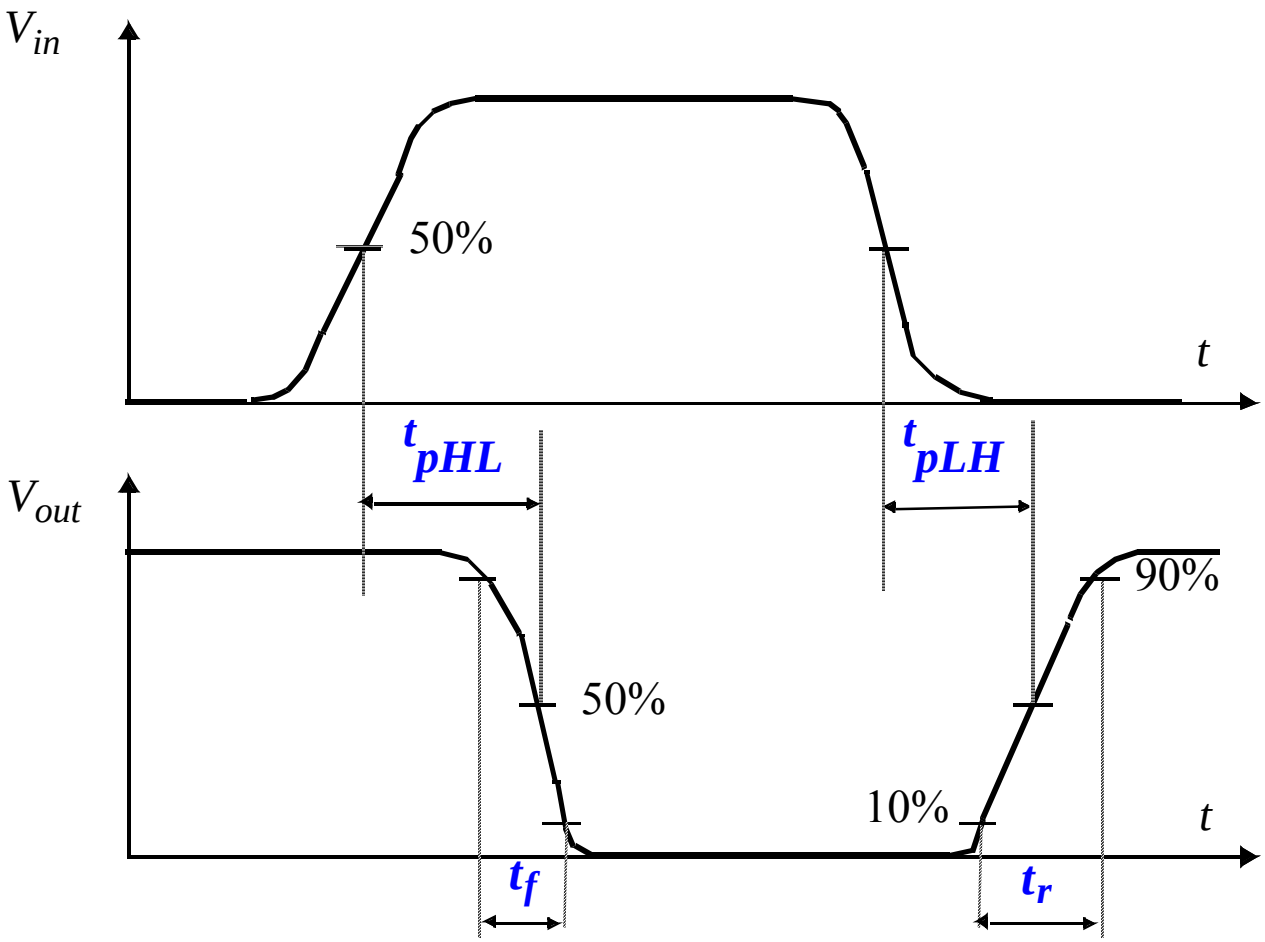

Figure 6 Transition Time Definitions

EE314 EXPERIMENT #4 DATASHEET

Date:

Name:

1)

λ_n (1/V)	λ_p (1/V)

2)

Kn (mA/V^2)	
Kp (mA/V^2)	
V_{thn} (V)	
V_{thp} (V)	

3)

Delay Times

tplh	tphl	tr	Tf

Capacitance (nF)
0.56
1.2
10