EE312 PROJECT # 1

DESIGNING A CMOS LOGIC CIRCUIT

Design a logic circuit layout using CMOS technology for the following function: Given an binary coded decimal input between 0 and 7, the circuit will produce an output that corresponds to the digits of your ID number. Here is an example:

binary inputs	7	6	5	4	3	2	1	0
digits of the ID#	9	6	0	4	6	0	6	0

That is, you will have three binary inputs (A, B and C) representing the decimal input and four binary outputs (w, x, y, and z) representing the decimal output between 0 and 9. You will determine the truth table for your own ID number, find the logic functions and then implement the layout using the layout tool **Magic**. Then, you will extract your circuit from the layout, and simulate with the **Spice** circuit simulator. The circuit must use 0-5 V power supply if it is composed of NOR gates or NAND gates only. It may use ± 5 V power supply if it is synthesized in minimum stage configuration. Note that, minimizing the area of the circuit layout will reduce the parasitic capacitances and impedances.

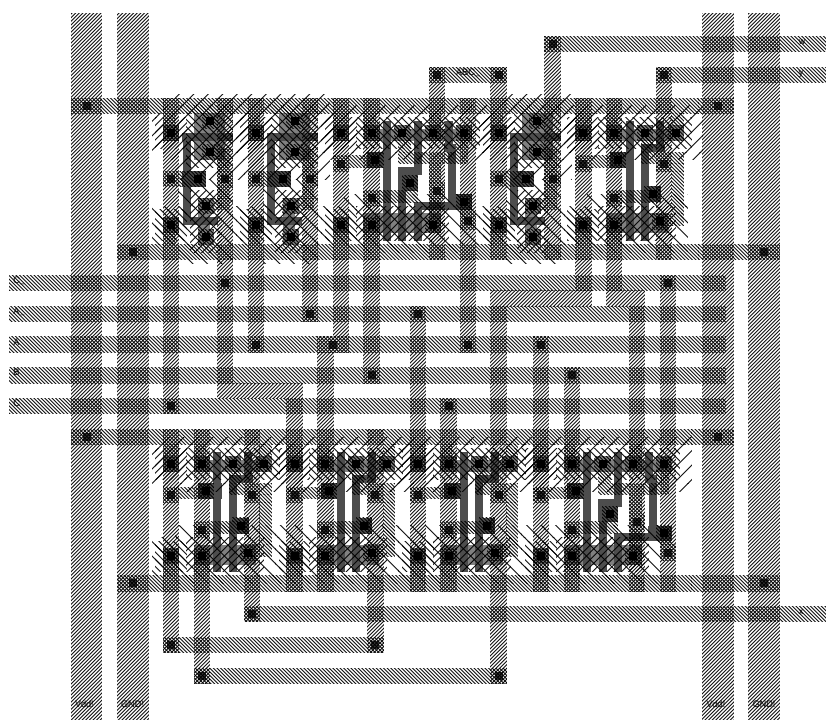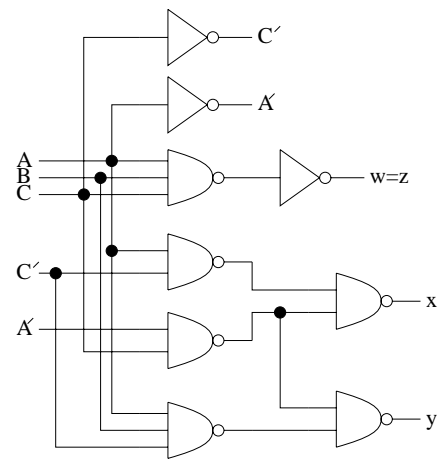As an example the truth table for the ID number above is formed as

decimal input	A B C	w x y z	decimal output
0	0 0 0	0 0 0 0	0
1	0 0 1	0 1 1 0	6
2	0 1 0	0 0 0 0	0
3	0 1 1	0 1 1 0	6
4	1 0 0	0 1 0 0	4
5	1 0 1	0 0 0 0	0
6	1 1 0	0 1 1 0	6
7	1 1 1	1 0 0 1	9

The above truth table has been implemented using a very basic layout with the **Magic**. The magic layout and the primary simulation results are also attached. As shown in the results for possible layouts, you may face problems like glitches during transitions and improper output levels which should be eliminated by further circuit modifications.

You are supposed to submit a circuit layout file and a brief report as an output of the project by May 3, 2002. After that You will be individually given an appointment date on which your layout file will be examined, extracted and simulated together with assistant.

Functions:

$$w = z \;\; = \;\;\;\;\;\;\;\; ABC \;\;\;\;\;\; = \;\; \overline{\overline{ABC}}$$
$$x \;\; = \;\; A'C + AC' \;\; = \;\; \overline{(\overline{A'C})(\overline{AC'})}$$
$$y \;\; = \;\; A'C + ABC' \;\; = \;\; \overline{(\overline{A'C})(\overline{ABC'})}$$