NOVEL PARALLEL LOSSY INDUCTANCE SIMULATION CIRCUIT EMPLOYING DO-OTA

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ABSTRACT

In this paper a new parallel lossy inductance simulator topology employing a single DO-OTA is presented. For the topology proposed, the inductance L_{eq} and the parallel resistance R_{eq} are independently adjustable. The topology employs a single capacitor and three resistors. Furthermore it is canonic in the number of capacitors. The resistors in the topology can easily be implemented also with DO-OTAs. In this case the topology proposed changes to DO-OTA-C-based inductor simulator which is important from the integration point of view. Simulation results are included to verify theory.

1. INTRODUCTION

Current-mode designs are accepted owing the possibility to operate at higher frequencies compared to the circuits employing op-amps. The current-mode analogue circuits employing active elements such as OTAs, current conveyors, DO-OTAs, DO-CCIIs, FTFNs play an important role in the IC design,since these active elements exhibit greater linearity and wider bandwidth and wider dynamic range over the voltage mode counterparts [1-13].

Actively simulated grounded inductors find applications ranging from filter to oscillator design to cancellation of parasitic inductances [3-9]. Many design possibilities are presented in the literature employing operational amplifiers, current conveyors, OTAs etc. as active element. The actively simulated inductors can be classified due to the type or the number of active and passive elements employed, if they simulate a grounded or floating inductance. Further comparison can be made whether they realise lossy or lossless types.

Although several circuits for realisation of immitance and inductance simulators have been reported in the literature, little attention has been paid to realising such type simulator circuits by using DO-OTAs.

In this paper a parallel lossy inductor simulator topology (parallel R-L) employing a single DO-OTA is presented. For the topology the inductance L_{eq} and the parallel resistance R_{eq} are independently adjustable.

2. DO-OTA

The circuit symbol of the DO-OTA is given in Fig. 1. Ideally, DO -OTA is assumed an ideal voltage-controlled current source and can be described by following equation,

$$I_0^+ = g_{m1}(V^+ - V^-)$$
$$I_0^- = g_{m2}(V^+ - V^-) \quad (1)$$

where I_0^+, I_0^- are dual output currents, V^+ and V^- denote noninverting and inverting input voltage of the DO - OTA, respectively.

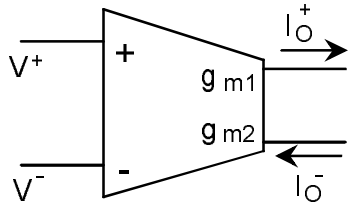
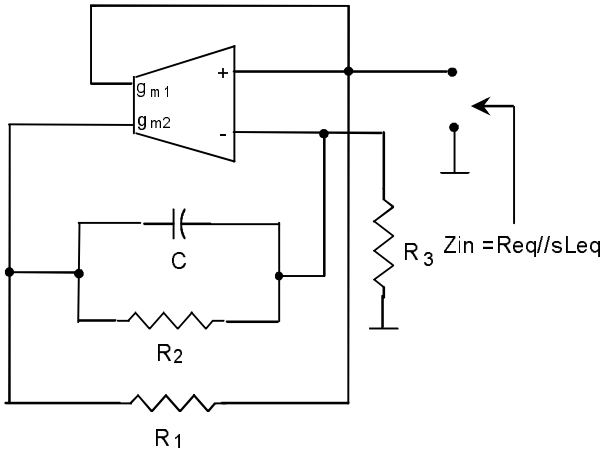


Figure 1. Circuit symbol of DO-OTA.



$$g_{m2} = G_2 + G_3 + \frac{G_2 G_3}{G_1}$$

$$g_{m1} > G_1 \quad , \quad g_{m1} = g_{m2}$$

$$L_{eq} = \frac{C.G_1}{G_2^{\,2}.(g_{m1} - G_1)}$$

$$R_{eq} = \frac{G_1}{G_2.(g_{m1} - G_1)}$$

Figure 2. Proposed DO-OTA based inductance simulator topology

3. THE PROPOSED CIRCUIT TOPOLOGY

The proposed lossy grounded inductance simulator topology is represented in Fig.2. The circuit was derived by using a systematic circuit generation method [14]. The corresponding equations for equivalent inductance and equivalent resistance are also given in Fig.2.

4. SIMULATION, DISCUSSION AND AN APPLICATION EXAMPLE

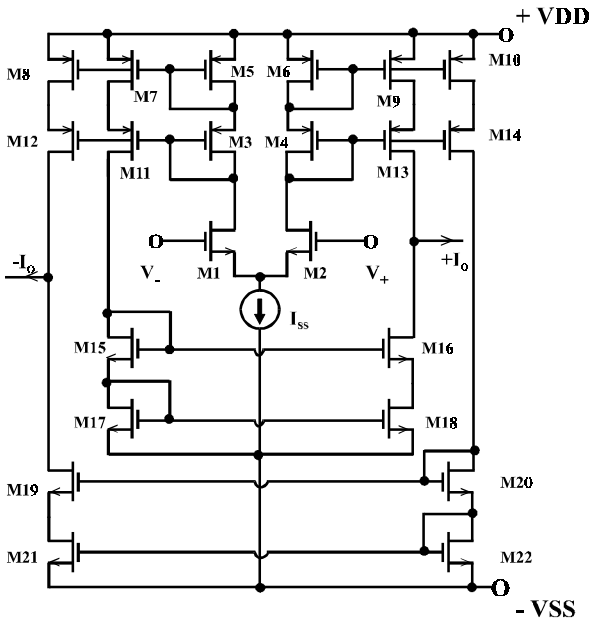


Figure 3. CMOS cascode DO-OTA structure used for SPICE simulations.

The circuit illustrated in Fig. 2 is tested with SPICE simulations. The test circuits were constructed with the CMOS cascode realization of DO-OTA illustrated in Fig.3 [13]. The SPICE simulations were performed with the high-accurate macromodel of this CMOS cascode DO-OTA [12].

To demonstrate the accuracy of the topology proposed, the frequency responses of the impedances obtained from ideal and simulated circuits are calculated. Furthermore a BP filter circuit was realized as an application example by connecting a parallel capacitor to the circuit illustrated in Fig.2. The circuit is designed to simulate a parallel R-L combination consisting of an inductor L_{eq}=2mH and a resistance R_{eq} = 1.25k. To obtain these values, the following values are chosen: $R_1 = R_2 = 5k\Omega$, $R_3 = 2.5k\Omega$ and $C = 0.32nF$. The DO-OTA transconductances are $g_{m1} = g_{m2} = 1mA/V$. The circuit was supplied with symmetrical voltages of ±10V. The frequency and phase responses of the impedances obtained for the ideal R-L circuit and for the DO-OTA-based inductance simulator are shown in Fig.4.

It can be easily observed from Fig.4 that ideal and simulated responses are in good agreement in a large operating range. Choosing the parallel capacitor as Cp = 2.59nF and driving the resulting parallel resonant circuit with current from a transconductance amplifier with a transconductance of 1mA/V, the frequency responses of the ideal and simulated BP filter circuits are investigated. The frequency response of the actual circuit obtained from SPICE simulations is given with the response of the ideal circuit in Fig.5. From Fig. 5 it can be easily observed that the SPICE simulation results obtained for the realization circuit are in good agreement with the results obtained for ideal parallel resonant circuit. The small deviation in the gain is caused by the non-idealities of the active element. Furthermore a 70 kHz and 200μA triangular wave current is applied to the input of the circuit and the waveform of the

voltage across the circuit is observed. The waveforms of the input current and the voltage across the circuit are shown in Fig. 6. Investigation of the circuit response shows that the actual circuit yields the expected sinusoidal waveform with an offset voltage. Note that this offset voltage is caused by the CMOS realization circuit and can be kept as small as possible by proper design of the DO-OTA.

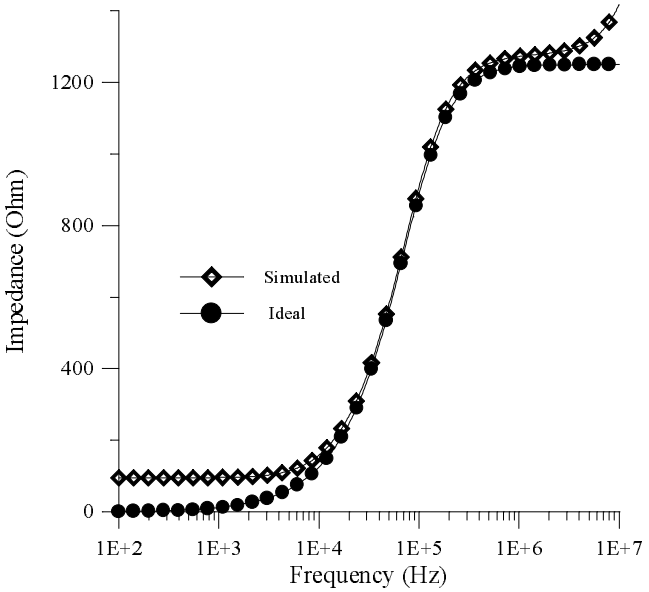


Figure 4. Plots of ideal and simulated impedance-frequency characteristics

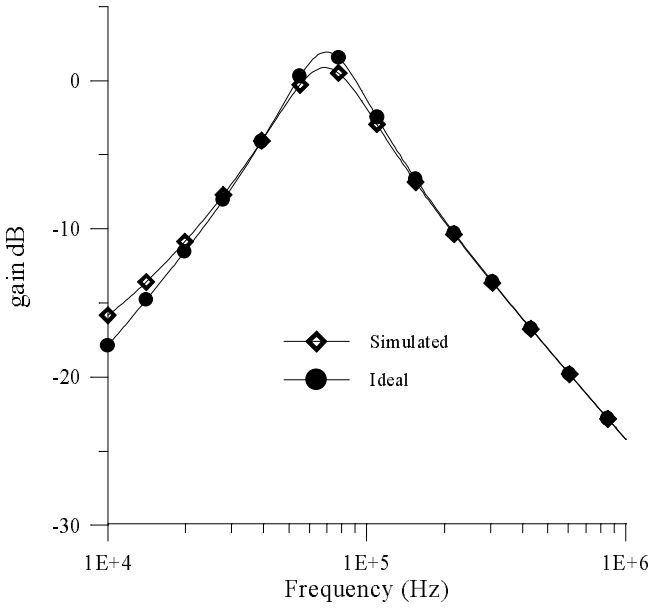


Figure 5. Frequency response of ideal and with DO-OTA simulated BP filter circuits

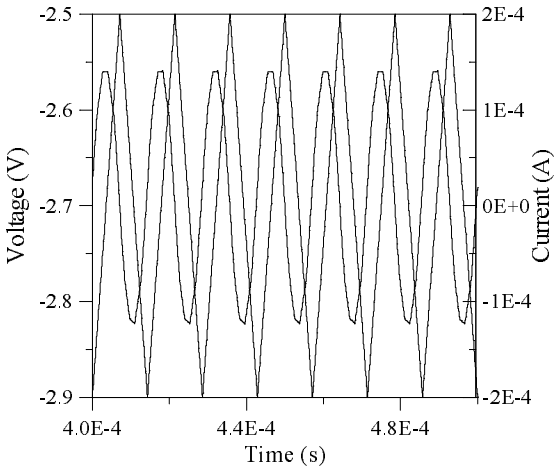


Figure 6. Transient response of simulated BP filter circuit to a 70 kHz triangular wave input current of 200μA.

5. CONCLUSIONS

In this paper an active parallel lossy inductor simulation topology employing a single DO-OTA is proposed. The resistors in the topology can be easily implemented also with DO-OTAs. In this case the topology employs only the same type active element which results in DO-OTA-C inductor simulators. Note that the realization with DO-OTAs and a capacitor is important from the integration point of view. This type of realization provides the IC designer the possibility of obtaining adjustable inductors since the DO-OTA transconductance can be easily controlled by the biasing currents. Simulation results are included to verify theory.

6. REFERENCES

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