QUANTUM-DOT CELLS AND THEIR SUITABILITY FOR NONLINEAR SIGNAL PROCESSING

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ABSTRACT

Electronics is more or less analog in nature, this applies to both the analog and digital circuits. Several transistors and other parts are needed for a single digital gate. However, this could change in the future. The concept of quantum computation has gained attention during the recent years, different architectures such as quantum-dot cellular automata (QCA) [7] have been proposed. Unlike normal electronics, QCA is fundamentally digital. In this paper we investigate the suitability of QCA architecture for nonlinear signal processing. Several examples are shown and the general usability of this concept is discussed.

1. INTRODUCTION

During the recent years there has been a growing interest towards quantum computing. It could bring significant improvements in speed, while the size and power consumption would decrease dramatically. However, it will take time before quantum computing is fully developed. At the moment it is a mainly theoretical concept, as there are many physical problems to be solved. Fabrication of such small structures is difficult, and one has to take many quantum mechanical aspects into an account. One possible way of realising such a system is based on quantum-dot cellular automata (QCA) [7]. They are an elegant way of transmitting and processing data using just two electrons for single bit. It is interesting to think, what kind of effects this new technology could have on many digital systems. Naturally, systems based on few molecules and electrons must have some kind of built-in error correction capabilities. However, the main point is that QCA forms a truly digital system. There can be only two stages, which can be considered as binary ones and zeroes. All normal logical gates are extremely simple and regular in this architecture. It is an ideal hardware for digital signal processing (DSP), and is especially well suited for many nonlinear digital filters, like order statistics or morphological filters. It is useful to think, how existing algorithms could be realised using this new technology. Majority logic and the uniformity of wires and processing elements brings many changes compared to traditional digital circuits.

2. QUANTUM DOT CELLS

Detailed explanation about the basics of this technology can be found from [11]. The basic block in QCA is a nanometre scale cell, which contains five quantum dots shown as circles in Fig. 1. Each cell contains two electrons. Coulombic repulsion between the electrons forces them to be located in the opposite corners of the cell. Electrons can change their location from one dot to another by tunnelling, thus the cells can have two different states corresponding to Boolean values of single bits. Nearby cells do have similar Coulombic interaction with each others. If one cell is set into specific a state, it tries to turn the electrons in neighbouring cells in positions, where all the distances are maximised. If these cells make a line, the electrons inside them will be aligned in a similar way [5]. This can be used for passing information in a same way as normal wire. Signal can be split as in Fig. 2.(a), or it can travel through corners.

Plus shaped formation of five cells shown in Fig. 2.(b) will behave as a logical gate. If three of the cells at the sides are fixed, the centre and remaining cell are forced in a same state as the majority of inputs. Majority logic gate is a basic block in this architecture. If one of the inputs is set into states 0 or 1, the remaining part of the cell will form logical AND, or respectively, OR.

Although QCA looks simple, there are many problems in the realisation of the actual circuits. Thermal noise can alter the state of different cells, the effect increases with the cell size and temperature. This and some other problems set limits for the maximum size of individual circuits, large circuits would switch into wrong states by themselves. However, the recent invention of using adiabatic pipelines seems to provide an answer for this problem [4]. Larger circuits can be split into many smaller ones, the size of each sub circuit is kept so small that thermal noise will not disturb the computation. Additional benefit is that the adiabatic pipelines make delay lines and finite state machines possible, this is essential for most algorithms. Detailed description of adiabatic switching and pipelines is rather long, we refer to [4], where this concept was first introduced.

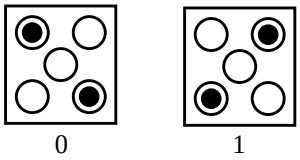

Figure 1. Different states of the basic cell.

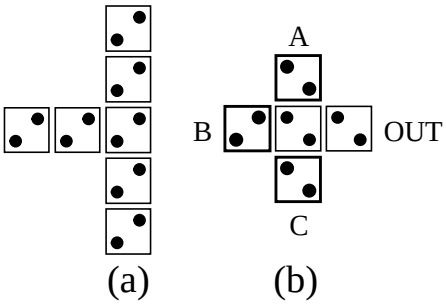

Figure 2. (a) Fan-out and (b) majority logic QCA structures.

3. QCA AND NONLINEAR FILTERS

QCA architecture is well suited for nonlinear signal processing algorithms [3]. Majority logic cell itself is a binary three point median. By using threshold decomposition and suitable sorting networks, it is possible to perform many typical nonlinear filtering operations in a simple manner. These include all order based filters such as different medians, L-filters, ranked-order statistic filters and stack filters, as well as morphological filters [1].

Lets look the odd/even transportation network shown in Fig. 3. This transportation network can be used for ordering samples from the smallest to largest, vertical bars denote comparators which place minimum value into one and maximum value into another output. This operation requires, that the signals have been split into binary vectors [6]. In that case the basic comparator units reduce to simple AND and OR gates, which can be realised using QCA cells as shown in Fig. 4. Note the turned cells used for crossings, and how they turn the polarity [10]. Black dots show, where the electrons are located with these input values. Cells forced to certain states are marked with thicker borders. By using a regular array of these basic units, one can realise all order based filters by selecting suitable outputs and weighting that is needed.

Majority logic can simplify many nonlinear filters. This would require nonlinear filter design algorithms, which can exploit the possibilities of majority logic. Regular structure of these cells would simplify the use automatic design tools.

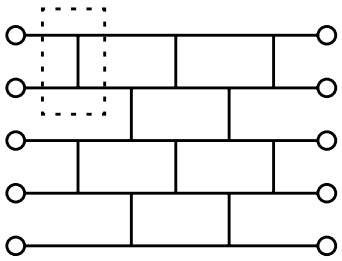

Figure 3. Odd/even transportation network. The vertical bars denote comparators.

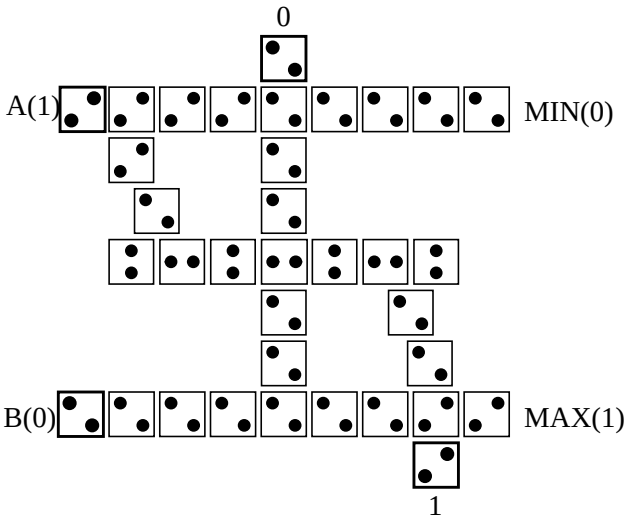

Figure 4. Comparator unit.

Examples of large nonlinear filters and grey scale image processing are difficult to construct, 8-bit data makes the circuits too large and complex. Thus, we have designed a simple noise removal filter for binary images. It is based on 3x3 pixel weighted median shown in Fig. 5(a). This filter can be given as a combination of 3-point medians, as shown in Fig. 6. If the middle pixel and at least one of the border pixels are equal, the pixel is kept as it is. If the middle pixel is different from background, it is considered as noise and it is removed.

It is not possible to show the whole circuit, we start from the point where the three consecutive lines have been separated. We need three pixels from each line, they are labelled as shown in Fig. 5(b). The first job is to construct delay lines, one needs three pixels from each row of the image. Delay lines can be constructed by exploiting adiabatic pipeline. Current pixels from each row are inserted into circuit from the upper left corner (Fig. 7), the starting point for these lines is not shown in this figure. It should be

(a) $\begin{bmatrix} 1 & 1 & 1 \\ 1 & 7 & 1 \\ 1 & 1 & 1 \end{bmatrix}$ (b) $\begin{bmatrix} a & d & g \\ b & e & h \\ c & f & i \end{bmatrix}$

Figure 5. (a) The mask for weighted median. (b) Pixels in 3x3 image block.

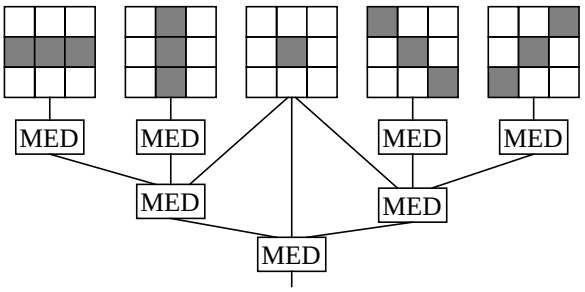

Figure 6. Weighted median of Fig. 5(a) as a combination of 3-point medians.

noted that the polarity of the rotated cells changes at each step, one has to select the connection point to normal cells carefully.

Different backgrounds for the cells refer to separate sub circuits, each of them is connected to one of the four different phases of adiabatic clocking device. Adiabatic pipeline has the property, that the bits separated by these four cycles are different from each others (in a similar manner as the neighbouring charges in CCD-cameras). By adding a suitable amount of these pipelines for signal path, one can create delays of desired size. In Fig. 7 upper pixels are delayed by two and the middle ones by one compared to low three pixels. It should be noted that these figures are not fully accurate, in the reality the cells do not change so suddenly from one state to another. We have not shown the effect of adiabatic cycles for the potential barriers inside the cells, it would make the figures too messy and impossible to follow without thorough understanding of [4].

After the delay lines all nine pixels are inserted into the actual filter circuit shown in Fig. 8. This circuit contains the seven 3-point medians shown in Fig. 6. Adiabatic pipeline has been used to divide the different stages from each others, this reduces ringing and thermal problems but it is not otherwise important for the functionality. Filtered output pixel comes out from the right hand side of the circuit.

We do not claim that this is the best or even a good structure for realising this circuit, perhaps the whole image should be filtered in parallel. We believe that this circuit would be functional, but we do not have the tools for the verification. It should be also remembered, that at the moment nobody can do the experiment with real hardware.

4. CONCLUSIONS

This new technology looks very promising, but it requires more advances in the physics, circuit and algorithm design. If these problems can be solved, it would have a great influence for nonlinear signal processing. Long computation time is a severe limit for many otherwise excellent nonlinear filters. It is possible that in the high speeds of quantum computation could these algorithms more practical for real applications. This is especially true for many computationally complex image, video, or radar signal processing applications. Many linear signal processing algorithms operating in transform domain would also benefit. It should be relatively easy to design scalable transform architectures using QCA.

The QCA architecture has gained more attention recently [2]. If there will be a breakthrough in this technology, it will have faraway consequences. One can use this technology for the realisation of traditional computers, but other kind of structures like CNN (cellular neural networks) are also possible [8],[9]. Esprit project DICTAM (dynamic image coding using tera-speed analogic visual microprocessors) dealt on new image compression methods based on a combination of signal processors and analog signal programmable processing arrays (ASPPA). This kind of work might be well applicable to QCA architectures.

We recommend the WWW-page http://www. mitre.org/ research/nanotech/index.html for those who are interested in quantum computation and especially QCA. This page contains a large amount of useful information and the current news from this research area.

REFERENCES

[1] J. Astola, and P. Kuosmanen, Fundamentals of nonlinear filtering. CRC Press, Boca Raton, p. 276, USA 1997.

[2] A. Hellemans, “Basic science,” IEEE Spectrum, pp. 100 - 103, Jan. 1998

[3] M. Helsingius, P. Kuosmanen, and J. Astola, “Nonlinear filters using quantum-dot cells,” Electronics Letters, vol. 33, no. 20, pp. 1735 - 1736, Sept. 1997.

[4] C. S. Lent and P. D. Tougaw, “A device architecture for computing with quantum dots,” Proc. of The IEEE, vol. 85, no. 4, pp. 541 - 557, April 1997.

[5] C. S. Lent and P. D. Tougaw, “Lines of interacting quantum-dot cells: A binary wire”, J. Appl. Phys. 74, pp. 6227 - 6233, Nov. 1993.

[6] I. Pitas, and A. N. Venetsanopoulos, Nonlinear digital filters, principles and applications. Kluwer, Norwell, p. 392, USA 1990.

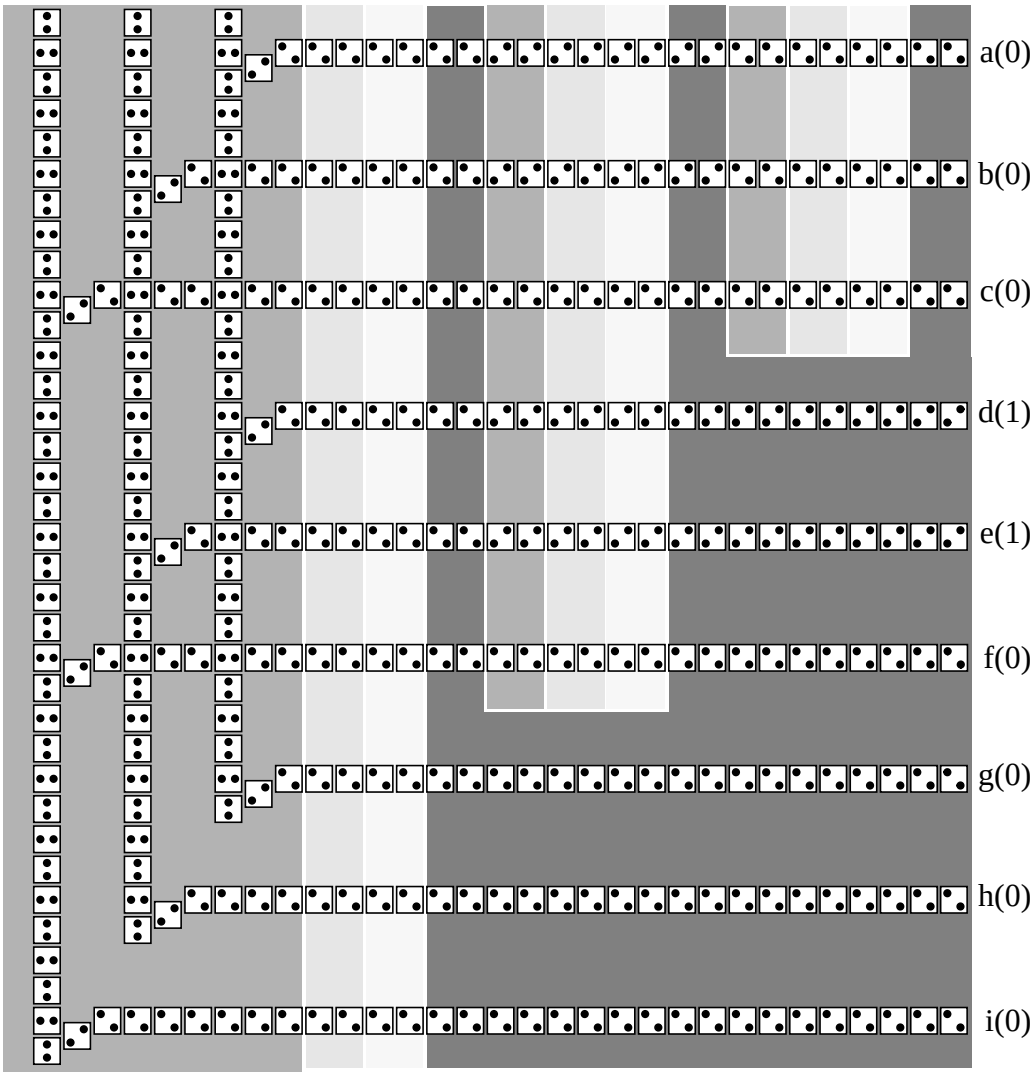

Figure 7. Delay lines of length 0, 1 and 2. New data is inserted into three vertical wires located in upper left corner, delayed outputs come out at right. Greyscale backgrounds refer to four different adiabatic pipelining cycles, responsible for actual delays. States for individual cells are drawn in simplified manner, this figure does not show the true location where the changes between consecutive bits occur.

[7] W. Porod, C. S. Lent, G. Toth, H. Luo, A. Csurgay, Y.-F. Huang, and R.-W. Liu, "Quantum-dot cellular nonlinear networks: Computing with locally -connected quantum dot arrays," Proc. IEEE Int. Symp. on Circuits and Systems, Vol. I, Hong Kong, pp. 745 - 748, June 1997.

[8] T. Roska, J. Hámori, E. Lábos, K. Lotz, L. Orzó, J. Takács, P. L. Venetianer, Z. Vidnyánsky, and Á. Zarándy, "The use of CNN models in the subcortical visual pathway," IEEE Trans. Circuits and Systems-I: Fundamental Theory and Applications, vol. 40, no. 3, pp. 182 - 195, March 1993.

[9] P. Thiran, "Influence of boundary conditions on the behavior of cellural neural networks," IEEE Trans. Circuits and Systems-I: Fundamental Theory and Applications, vol. 40, no. 3, pp. 207 - 212, March 1993.

[10] P.D. Tougaw and C. S. Lent, "Logical devices implemented using quantum cellular automata," J. Appl. Phys. 74, pp. 1818 - 1825, Feb. 1994.

[11] P.D. Tougaw, C. S. Lent, and W. Porod, C. S. Lent, "Bistable saturation in coupled quantum-dot cells," J. Appl. Phys. 74, pp. 3558 - 3566, Sep. 1993.

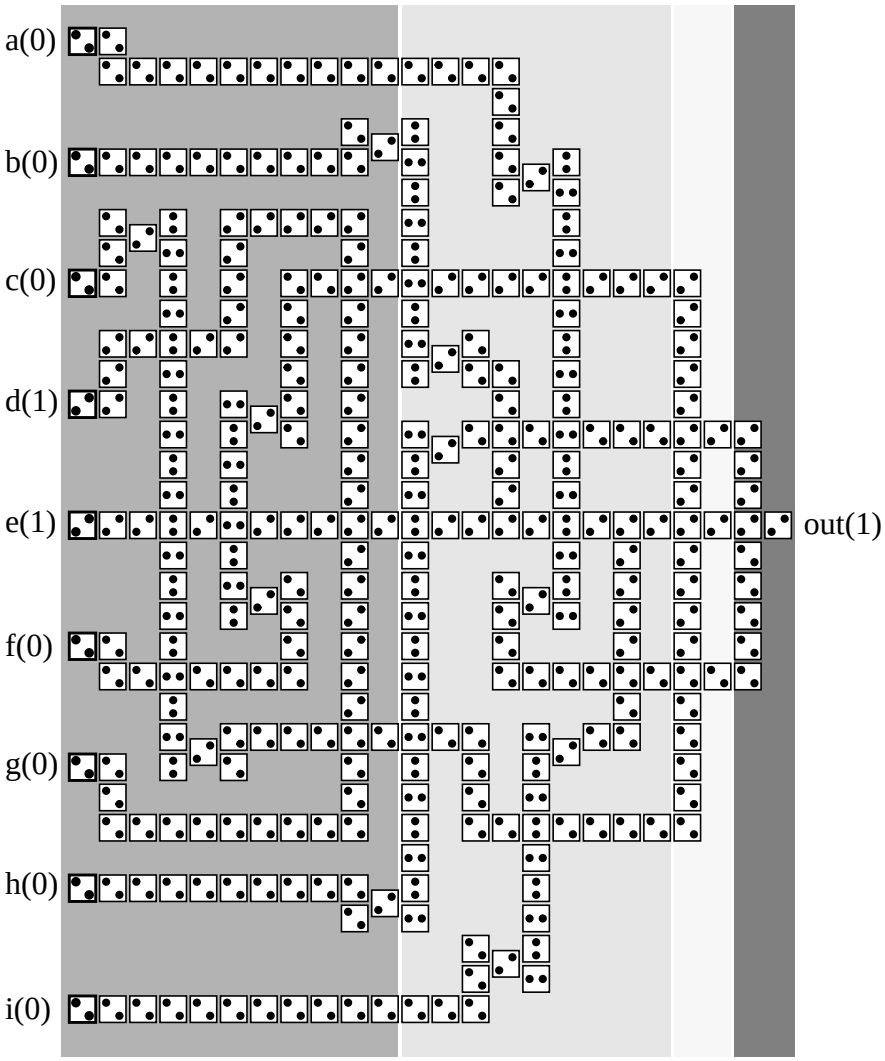

Figure 8. Weighted binary median for 3x3 window. The filter is realised with a combination of 3-point medians. Adiabatic pipeline has been used for dividing the circuit into subcircuits, delays are not used.