SIMULATION AND APPLICATION OF DVB CHANNEL CODING ON MULTIMEDIA DSP DEVELOPMENT BOARD

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ABSTRACT

This paper deal with the simulation and application of DVB channel coding on multimedia DSP development board uses Nexperia processor. The application provides the protection against errors during the transmission of real digital video by the transmission channel model in baseband. Applied codes present FECs protection (forward error correction codes - RS code, convolutional code, interleaving) and the channel model causes defined pertubation and distortion of transmitted data. There are presented flowcharts of developed and applied algorithms, experimental results and presentation of DSP based demonstration applied to real digital video in this paper.

1. INTRODUCTION

Channel coding of digital video data stream and utilization of error correction codes is defined in DVB (Digital Video Broadcasting) standard. The principal of the transmission with error-protection coding in digital television deals with the redundancy information that is added to the source-coded digital signal in the channel encoder. This enables the channel decoder in the receiver to correct any errors. The task of channel coding in the receiver is to find the position of the incorrect bits by the evaluation of the redundancy that is also possibly affected by the transmission errors. System that can evaluate the efficiency of protection codes on real digital video and its quality can be hardware implemented in laboratory using multimedia DSP. This work proceeds with the previous simulation applied in Matlab and presented in [1].

2. CHANNEL CODING IN DVB STANDARD

Two relevant methods of error protection in the transmission of digital video and digital television accords to standard DVB [2] are FECs (forward error corrections) by block Reed-Solomon code (FEC1) and convolution code (FEC2) with interleaving. The RS (255, 239) was chosen which processes a data block of 239 symbols and can correct up to 8 symbol errors by calculating 16 redundant correction symbols. As an MPEG-2 packet is 188 bytes long, the code was shortened, i.e. the first 51 information bytes were set to zero and not transmitted at all. In this way the RS (204, 188) code is generated. After the outer code a convolution inter-

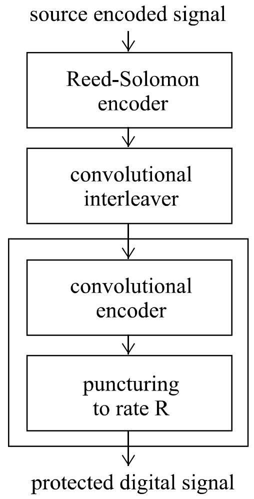

Fig. 1 FEC codes in the transmission of the DVB.

leaver with depth I = 12 is used. From the frame length of the outer code with n = 204 the base delay results as $M = n/I = 17$. Finally a convolution code is applied to the interleaved symbols. Its rate $R = m/n$ - where m is the number of input bits and n of output bits - is equal to 1/2, the constraint length is $K = 7$.

3. CHANNEL DECODING ALGORITHMS

3.1 FEC1 decoder implementation

The RS code (FEC1) is symbol oriented code. The correction is not only in the error recognition and its replacement. Symbol with the error should be replaced. The symbol protection deals with the finite set of numbers and its arithmetic uses Galois field. The decoder (in Fig. 2) [3] deals with the word $v(x)$ that was received after the transmission. The code word $c(x)$ is overlaid with the errors that are represented by the word $e(x)$ (all words are in polynomial representation). The polynomial of received code can be figured out in roots of generator polynomial $g(x)$ used in transmitter and these roots are the powers of primitive element α. Computation of syndrome $S(x)$ means enumeration of $v(x)$ in powers of primitive polynomial α. The syndrome contains the location numbers and unknown values of errors.

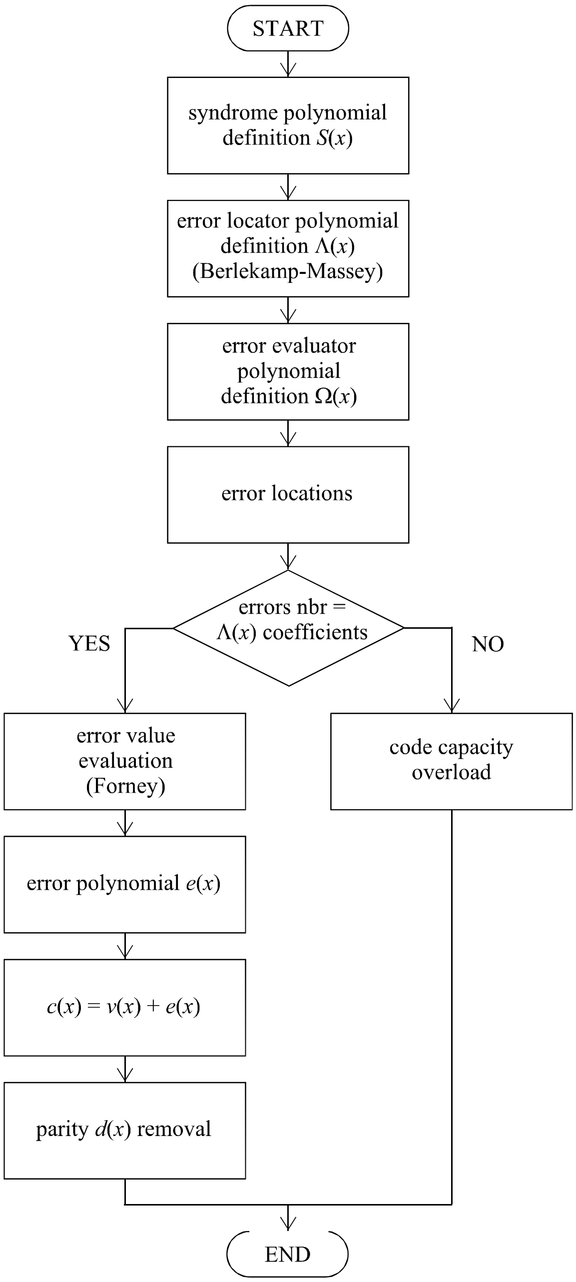

Fig. 2 Implemented FEC1 decoder flowchart diagram.

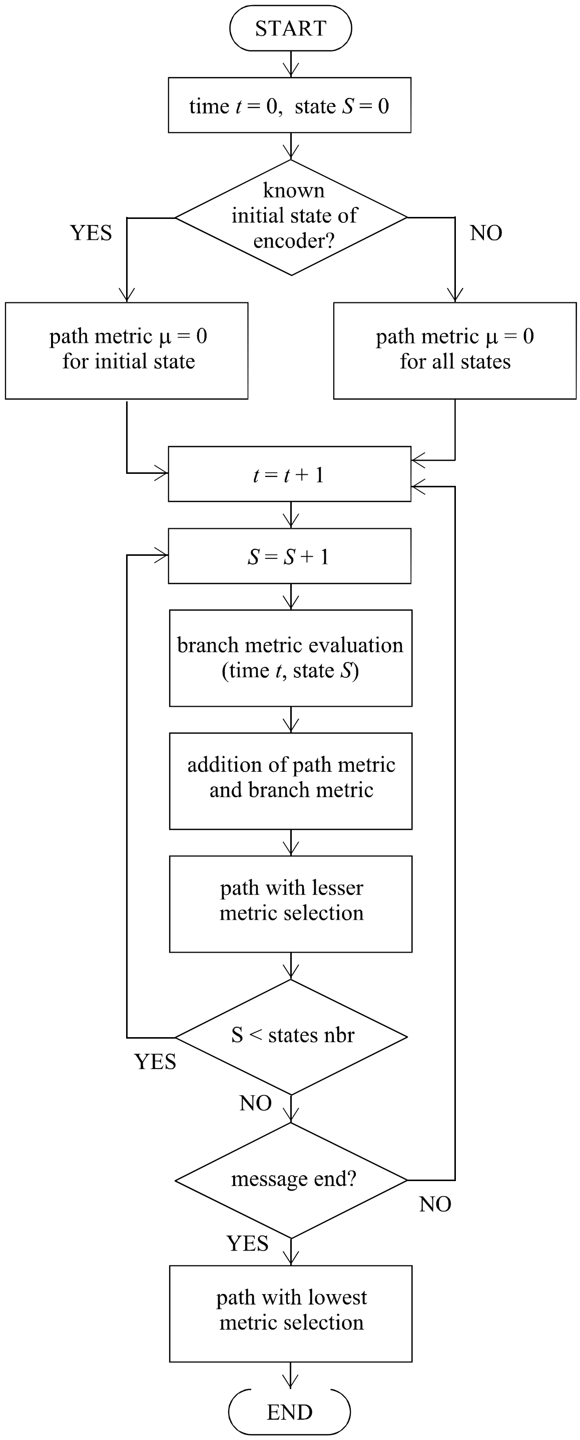

Fig. 3 Implemented FEC2 decoder flowchart diagram.

Error locator polynomial $\Lambda(x)$ roots are the inversion of location numbers. The error evaluator polynomial $\Omega(x)$ is exactly related with the position and value of single errors. The error locator polynomial method evaluation uses iterative technique in approximation of the locator polynomial. The values of errors are obtained by Forney algorithm that operates with the $\Lambda(x)$ and $\Omega(x)$. With the knowledge of the error values and error position the error polynomial $e(x)$ can be evaluated. After the errors removal the parity check could be done. If the number of errors is not equal to error locator polynomial coefficients the code capacity is overload and the decoder will fail [4].

3.2 FEC2 decoder implementation

The convolution code (FEC2) is binary oriented and correction of binary errors is possible only with the bit inversion after the error localization. Efficiency of convolution code depends on the length of used shift register in coder and its content determines the state of coder. Viterbi algorithm of the decoder (in Fig. 3) [3] is wide-spread decoding technique of convolution codes.

Decoder receives the code sequence and creates estimated message *v*' of code word *v*. This estimation minimizes the Hamming distance between the received sequence *r* and transmitted sequence *v* (seeks such code word that is different at least positions). To find this code word the trellis diagram is searched through and the paths that don't lead to minimal Hamming distance are removed. Only one path is reserved for one state in each moment. If the coder was in initial state, only one path remains after the search. If the initial state is unknown, the path with the minimal Hamming distance is selected. The branch metric is evaluated for each time t and each state $S(t)$ and it is equal to Hamming distance of received bit sequence to the other sequences in the same state. The path metric μ for each subsequent state $S(t)$ is equal to sum of the branch metric and the path metric of previous state $S(t-1)$ [5].

4. DSP DEVELOPMENT BOARD

The MDS TM-13 IREF [6] is a PCI bus board for real time video, audio and telecommunications signal processing. It uses the 180 MHz Philips PNX-1300 DSP processor [7] (called Nexperia) that is 32 bit fixed and floating point VLIW processor with integrated video and audio interfaces. The development board provides video I/O in both CVBS and Y/C formats and stereo audio I/O. The Nexperia processor is programmed in C or C++ using compiler that include operations for efficient real time video processing. The DSP also has a built image co-processor and variable length decoder (VLD) used in MPEG video compression.
The Nexperia processor operates with the IADK application libraries. These are basic input and output video and audio codecs. The libraries are available option used with the development board and it also contains MPEG (Motion Picture Expert Group) encoders and decoders [8]:

- *MPEG encoder and decoder Lib* (according to ISO/IEC 11172-2 and 13818-2) - provides a set of functions produce the MPEG-1 video streams from pictures separate from YUV (4:2:0) pixel data blocks, I and P – frames support, variable/constant bit rate, free definition of quantizer, MPEG decoder accepts the MPEG-1 and MPEG-2 MP@ML,
- *MPEG program and transport stream demux Lib* (according to ISO/IEC 11172-1 and 13818-1) - extracts the stream of MPEG audio and video, recognizes the IDs of streams and corresponding PES (Packetized Elementary Stream) start codes and parses PES packets, the demultiplexer receives a single MPEG-2 transport streams, scans the incoming PES, extract the PIDs of video and audio and starts to decoding stream.

Generally, the MPEG family standards are used as an effective tool for coding audio and video signals. The MPEG-1 and MPEG-2 may both reduce the temporal correlation so that a greater coding efficiency is achievable. Used libraries present standard solution of multimedia and digital video compression.

5. DIGITAL VIDEO CODING, COMPRESSION AND TRANSMISSION IN LABORATORY

The setup of experimental transmission of digital video in laboratory is in Fig. 4. The video source is standard camera with the analog video output connected to DSP development board that has integrated ADC encoder SAA7121. After the conversion the digital video samples YUV are available. The output digital video is converted by the DAC decoder SAA7113 and analog output is displayed on any AV monitor. The DSP development board is forced by the PC and NDK (Nexperia Development Kit) including the MPEG libraries operates in real time. The FEC1 and FEC2 encoders and decoders are external modules and provide the channel coding of multimedia and packet data video stream [3].

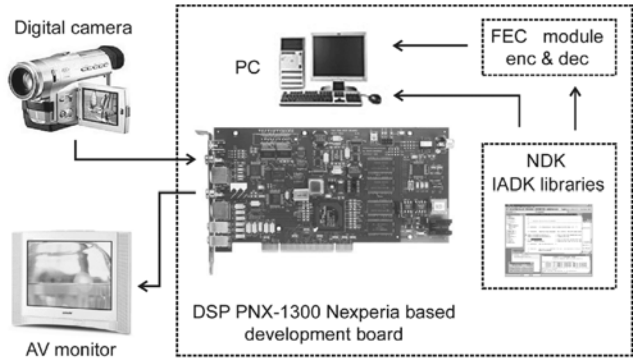

Fig.4. Illustrative setup of experimental digital video transmission in laboratory.

The development board operates with the video input and reads digital video data stream from an off-chip source into main memory, it accepts CCIR656-compliant device with 8-bit parallel 4:2:2 YUV. The video output provides a digital YUV data stream to off-chip video subsystems vice-versa to video input. Gathering bytes from the separate Y, U, V planes stored in SDRAM generates the output signal. The image coprocessor unit off-loads the CPU of cycle-consuming image processing tasks such as copying image from SDRAM to a host video frame buffer. The VLD unit operates as a memory-to-memory coprocessor to decode Huffman-encoded MPEG-1 and MPEG-2 video data streams [9].

6. EFFICIENCY OF THE CODES RESULTS

Although the RS codes are symbol-oriented codes [4], the analysis of the efficiency takes bit errors into account. The efficiency of the code increases with an increase in the number of test symbols. At an input bit-error rate of 2.10^{-3} the residual bit error rate of the RS (255, 205) code is approx 1.10^{-10} - the coding gain is thus more than 10 to the power of 7 - whereas in the case of the RS (255, 239) code at the same input bit-error rate the output bit-error rate is 9.10^{-4} - the coding gain is only slightly greater than 0.5.

For all DVB transmission standards a modified (shortened) RS (255, 239) code is used which makes it possible residual bit-error rate of approx 1.10^{-11} at an input bit-error rate of 2.10^{-4} while correcting up to 8 symbol errors per block. The residual bit-error rate of convolutional codes [5] of rate R is a function of E_b/N_0 (energy transmitted per bit divided by the noise-power density of the white Gaussian noise) and the parameter K describes the length of the code. The performance of the error correction increases with increased K. For the DVB standard a convolutional code of rate $R = 1/2$ with a constraint length $K = 7$ is used. With $E_b/N_0 = 3.2$ dB it is possible to achieve a bit-error rate of less than 2.10^{-4} at the output of the decoder, this ratio corresponds to the maximum of the bit-error rate at the input of the RS decoder, so finally a bit-error rate at the output of the RS decoder of less than 1.10^{-11} is obtained.

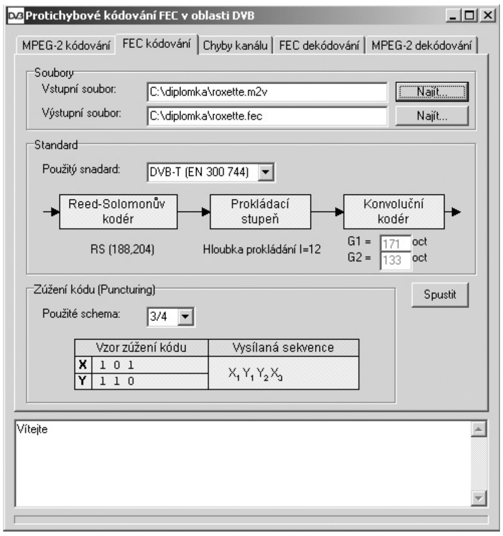

Fig.5. Control panel of developed application for DVB channel codes parameters (example in Czech).

7. CONCLUSION

The experimental application of channel coding of multimedia digital video using DSP development board TM-13 IREF was presented in this paper. The control panel of developed programme is in Fig. 5 [3]. There is possibility of DVB standard selection from S, C to T, input and output file specification, parameters of used error correction codes (RS, interleaver and convolutional code + puncturing). Described transmission uses the model that makes definition of the random errors of the digital data and low-pass filtering. The filter is modelled as a FIR filter with variable attenuation, cut-off frequency and filter order and it is used for filtering of MPEG-2 compressed video data stream in baseband. The channel coding provides the resistance against errors during the transmission of coded video data. These errors are occurred in transmission media and they are usually caused by any perturbation. The observer can evaluate the errors on the AV monitor screen in spatial area (visual information) and the subsequent subjective evaluation of video quality is possible (see Fig. 6). Due to block based MPEG-2 compression the image artefacts are easy visible according to amount of errors that are imposed on transmitted packets of digital video stream. The channel model parameters have not been discussed yet. The model of the perturbation should be defined more exactly (limited bandwidth) and motivates to future research work.

Fig.6. I-frames of MPEG-2 video a) with and b) without the error protection and LP filtering of digital video stream (example).

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