MULTI-STANDARD DEVELOPMENT AND MEASURING PLATFORM FOR MIMO-SOFTWARE DEFINED RADIO

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ABSTRACT

The demand for ever higher speed mobile communication is one of the main drivers of the telecommunication industry. A promising method capable of achieving high data rates is multiple input – multiple output (MIMO) technology, which has the potential to increase capacity linearly with the number of antennas. The development and measurement platform presented in this paper will simplify the design process of communication systems based on MIMO or smart antenna technology. It is compliant to GSM, UMTS and WLAN standards. In particular the development of software defined radio systems (SDR) is simplified and needs no system changes for supporting each of these standards. Moreover, the system is a flexible testbed for MIMO channel experiments and measurements. It comprises a multi channel receiver for implementation of a SDR and a MIMO channel simulator for evaluation of MIMO or smart antenna algorithms.

1. INTRODUCTION

Multiple input – multiple output (MIMO) techniques are a determining factor in future communications systems. They offer significant improvements in spectral efficiency and reliability. However, MIMO algorithms are rather complex, making their implementation in hardware difficult and erroneous. Since redesigns are quite costly (approx. 1 million USD per redesign [1]), it is desirable to detect and eliminate fundamental errors early in the design of a MIMO chip.

The primary purpose of the described development platform is the assistance in building software defined radio systems (SDR) and prototypes. It can also be used for validation of end-to-end transmission scenarios. With its built-in real-time channel simulator, the development platform is able to carry out dependable, unlimited in time and reproducible real-time simulation. It therefore reduces costs to a high amount, since there is no need for time consuming field tests.

The platform is based on a versatile digital signal processing (DSP) board featuring a synergetic combination of a flexible DSP as well as a highly parallelized field programmable gate array (FPGA). The platform is assembled with up to ten DSP boards to gain the required performance (see Figure 1). A mature feature is the support of rapid prototyping and hardware in the loop. So, designing and validating algorithms can be performed efficiently, resulting in shorter development cycles and lower costs.

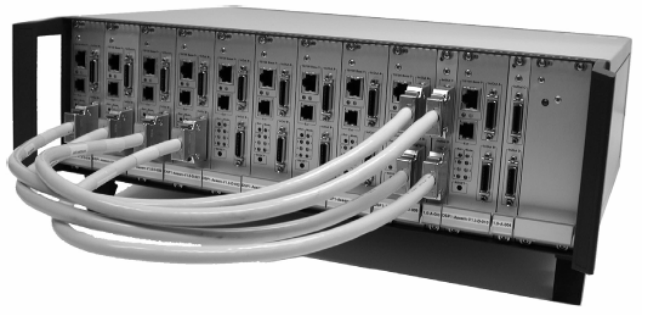

Figure 1: Development platform

Other development platforms exist for MIMO communication [2]. However, they are based on real MIMO transmissions and thus simulations cannot be reproduced. On the other hand, the real-time hardware channel simulator described in [3] is able to reproduce simulations, but only for a limited number of timeslots. Further the platform doesn't provide development boards for rapid prototyping.

The rest of the paper is organized as follows. The core of the development platform – the DSP board and its analogue interface is presented in Section 2. An architectural overview of the development platform is provided in Section 3. Information on the channel simulator is given in Section 4. Section 5 presents the MIMO receiver and the rapid prototyping methods. Finally the practical features of the development platform are demonstrated in Section 6.

2. DSP-BOARD

2.1 Baseband Processing

The base of the development platform is a DSP/FPGA signal processing board offering high processing power and a multitude of interfaces; especially LVDS (Low Voltage Differential Signaling) interfaces for transmitting baseband signals at highest possible clock rate (see Figure 2). This signal processing board forms the base for implementation of the MIMO receiver as well as for the MIMO real time channel simulator.

The DSP TMS320C6416 (600 MHz- or 1 GHz- version) with its built-in Viterbi decoder is tailored for calculation of complex MIMO tasks. The FPGA XC2V2000 from XILINX with its 56 built-in 18 x 18 multipliers is used for I/O interfacing and for fast calculation tasks, which are suitable for

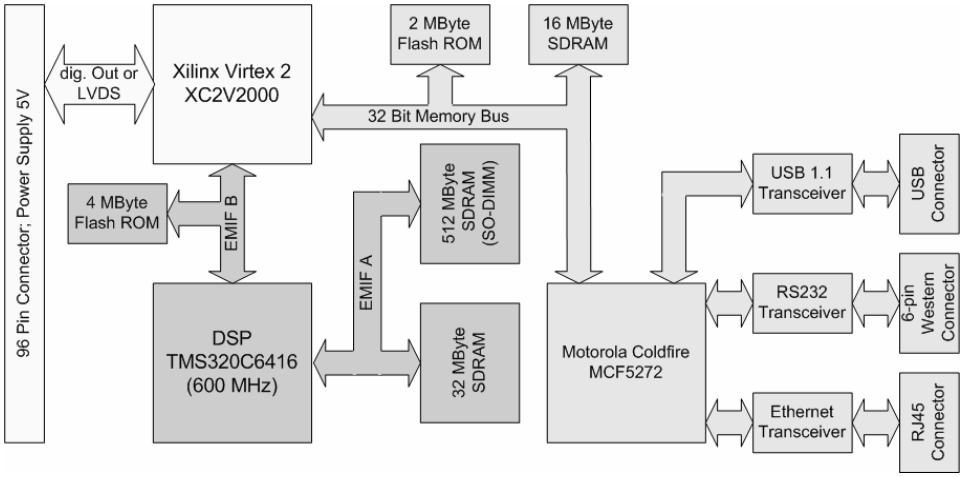

Figure 2: Block schematic of the DSP board

parallelisation. For example, for the channel engine of the channel simulator, 24 calculation paths have been designed to carry out identical calculation steps (superposition of several signals) simultaneously. With its 624 flexibly configurable I/O pins, the FPGA manages internal signalling (busses, control) as well as external data exchange to comply with different interface standards. Six LVDS transmitter/receiver units have been implemented in the FPGA for transmission/reception of LVDS output/input data.

In addition to the two chips dedicated to data processing a Motorola „Coldfire" MCF5272 microprocessor is available on the board. Its Fast Ethernet interface makes it possible to configure each board easily from a PC. The Coldfire runs a tailored version of µClinux for a convenient implementation of the UDP and TCP/IP protocol. By moving a part of the development tools to the Coldfire, it is able to re-configure the whole system on-line.

2.2 Analogue Processing

Each DSP-board can optionally be equipped with an analogue frontend. It comprises a digitizer and a D/A converter plus a FPGA XC2VP30, which handles I/O interfacing, digital mixing, and controlling of the board (see Figure 3). The digitizer is built by two ADS5500 from TI and under samples the IF signal at a sampling rate of e.g. 112 MSPS using 14 bits. Direct sampling of the 140 MHz IF reduces errors associated with analogue processing – in particular I-Q balancing is nearly perfect. The digitized signal is digitally mixed down into digital baseband. The complex mixer is implemented inside the FPGA and uses a arbitrary oscillator frequency, so it is not restricted to a frequency of $F_S/4$, where F_S is the IF frequency.

The A/D converter uses a two-channel DAC5686 from TI operating with 16 Bit. It has a selectable interpolation filter for oversampling factors of 2 to 16 and an integrated complex digital mixer for shifting the signal to IF range before converting it into an analogue signal.

The clock and the SYNC signal have to be synchronous for all analogue boards. To gain this synchronisation, two splitters for the clock and the SYNC signal are used, which are housed in a separate rack. One analogue board generates the clock and the SYNC signals, which are fed to the splitters and are directed by wires with equal length to the individual boards.

3. OVERALL PLATFORM ARCHITECTURE

The performance required for multi channel reception or channel simulation is acquired by up to ten DSP boards, which are accommodated in a 19" rack. The radio frequency (RF) parts of the frontend are separated from the rest of the system and reside in an own rack to reduce influences on the system.

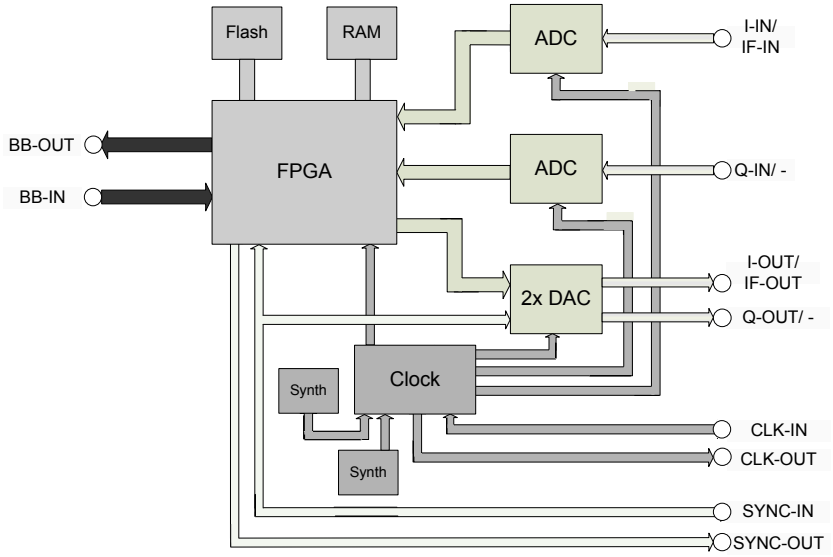

Figure 3: Block schematic of the analogue board

3.1 Data Communication

To forward partial results and distribute input signals, a powerful data communication between the boards is essential and is established by a backplane with fixed wired LVDS connections.

The LVDS connections are based on the ChannelLink specifications for 32 bit signals providing a maximum of 1800 Mbit/sec/link. Each DSP board comprises six LVDS transmitters/receivers. Four LVDS channels are used as inputs and outputs respectively using standard CameraLink connectors. Two are accessible at the rear side and two at the front side of the rack. The other two LVDS channels are

linked with LVDS channels of the previous and next DSP board over the backplane, resulting in a daisy chain.

Two DSP boards and two extension boards (providing additional LVDS input channel connectors at the rack's front that are directly routed to the backplane without any processing) form a separate block. They are designed to be used for data acquisition and processing, such as a MIMO receiver.

3.2 RF frontend

One RF frontend (1 transmitter and 1 receiver) plus one analogue board convert one MIMO RF channel into a baseband signal and vice versa. The RF frontends are separated from the rest of the system and reside in an own rack identical to the rack of the platform to reduce influences on the system. Both the transmitter and the receiver are implemented on a separate board. The first version of the RF receiver is designed for WLAN signals only and operates with input signals in the frequency range from 5,15 to 5,25 GHz.. Extensions complying GSM and UMTS standards are planned for the next version. The receiver has a two staged down converter to 140 MHz intermediate frequency (IF) with four different IF filters, selectable by a pin-diode switch and corresponding to the different bandwidths (maximum of 56 MHz) of the individual wireless standards. The first IF filter has a centre frequency of 947 MHz and a fix bandwidth of 56 MHz.

In the RF transmitter, the analogue IF signal is upconverted following the same frequency plan as the downconverter of the receiver. Two local oscillators, which are programmable in steps of 20 kHz, are assembled on a separate print and their signals are distributed to all RF boards. The LO signals have to be synchronous for all RF boards. A similar approach is used as for the analogue boards. The two LO signals are fed to two splitters in a separate rack and are directed by cables with equal length to the individual boards.

4. MIMO CHANNEL SIMULATOR

The MIMO channel simulator is assembled by several DSP boards each simulating one link of the MIMO channel. Thus for an n → m MIMO scenario, n • m boards are required. Following MIMO systems can be realized by use of one rack: 1→8, 2→2, 2→4, 4→2, 8→1. For larger MIMO systems cascading of up to eight racks is possible, so the maximum is an 8 → 8 MIMO scenario. The bandwidth of one baseband signal can have up to 30 MHz.

The input signals are generated by an internal GSM/UMTS/WLAN Modulator or fed into the BB input connectors at the front panel, replicated and distributed to the corresponding boards by patch cables at the rear side of the system. The output signal of each board of a group is routed through the LVDS daisy chain at the back plane to the next board, which adds the signal to its own simulation result, and outputs the sum signal. So the result of each group is given in the last board of that group and directed to the front side output connector of this board.

Each board of the simulator calculates the propagation process for one link of the MIMO channel. The simulation is based on parameters of a built in channel model according to COST 259, which are provided by a graphical user interface [4][5]. As an alternative, user defined channel models can be integrated into the system. Two different forms are applicable for the user defined channel model: Either channel sounder data or an analytical representation of the impulse responses as a XML file can be chosen. The impulse responses can hold up to 24 paths, which have a arbitrary delay. So the corresponding scatterers of the model are not restricted to an equidistant structure. The XML file is converted in Matlab and directly fed to the channel simulator.

The simulation is split into the calculation of the individual signal components incident on one receive antenna and in the superposition of these components [6]. The first part is carried out by the DSP, which has to do complex geometrical and stochastical calculations. The superposition is a task suitable for parallelisation and is therefore done in a separate module inside the FPGA, the "Channel Engine". The Channel Engine operates with 24 calculation paths (enhancement to 48 is planned).

The channel simulator can also be used as a MIMO Signal Generator, which forms MIMO signals from the internal modulation signal.

5. MIMO-RECEIVER

The platform's receiver unit comprises two DSP-boards and two extension boards providing additional LVDS input connectors at the front of the rack. Alternatively, the analogue boards can be used at the receiver side providing two analogue inputs for each board. So the receiver can operate with a maximum of eight input BB signals or up to four analogue input signals.

With the support of rapid prototyping and hardware in the loop, designing and validating algorithms can be performed efficiently, resulting in shorter development cycles and lower costs [2]. A "Golden Code" is designed in Generic C, which is primary C language enriched with predefined keywords for interfacing. The mapping tool GenC maps Generic C algorithms into C code for the receiver or into Simulink S-functions. An automatic partitioning of blocks to the DSP or to the FPGA is supported by the tool. The receiver can also be integrated into Simulink working as a "hardware in the loop" [1]. The tool GenCAddon extends the C-code with initialize, transmission and reception routines. So it is possible to co-simulate algorithms in Simulink as well as on the targeted hardware.

For demonstration purposes, we implemented a real-time Smart Antenna receiver for the GSM mobile standard. The receiver operates in digital baseband domain. It uses the MDIR (Matched Desired Impulse Response) algorithm [7] to calculate the combiner weights at the antennas. A detailed description of the algorithm and simulation results can be found in [8].

6. THE DEVELOPMENT PLATFORM IN PRACTICE

For designing first algorithms, implementation of a MIMO system, channel measurements or evaluation of complete systems, this platform represents a useful tool. Early elimination of fundamental errors reduces the number of redes-

igns necessary. MIMO algorithms can be easily implemented on the receiver and evaluated immediately with the channel simulator. Figure 4 shows a 2 → 4 MIMO configuration of the platform operating with BB signals. Eight boards are used for channel simulation and one board (with additional LVDS inputs) is used as a receiver.

Both the receiver and the simulator are controlled by the GUI (Graphical User Interface) on a PC. The GUI stores the user's configuration of channel simulator parameters, controls the channel simulator and stores simulation results. Before starting the simulation, the GUI uploads the standard-specific programs to the DSP and the FPGA of each simulator board. The input signals to the simulator originate either from an external source (baseband or analogue) or are generated by the internal modulator. The simulator distorts the signals according to the used channel model and outputs them either as baseband or analogue signals.

Further, online reconfiguration of the system is possible. The flash memory of the DSP of each board holds two different versions of configuration files (each file comprises the configuration for both the DSP and the FPGA, which are allocated to different memory sectors). The switching between these two configurations is triggered by a GUI command and booting is performed within one second. So, various versions of any receiver module can be compared easily.

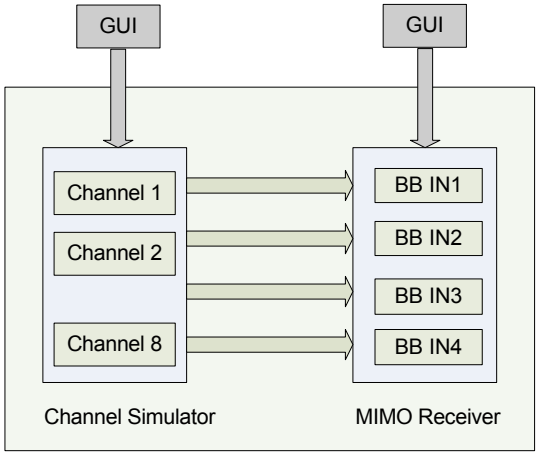

Figure 4: 2 - 4 MIMO platform

The platform is further ideally suited for use as a channel sounder. The transmitter signal is generated by the internal GSM/UMTS baseband modulator and converted into RF band by the analogue and RF boards. The reception data are converted into baseband and stored in the huge memory of the platform. The FPGA collects the data and saves them in the 512MByte memory of the DSP. After termination of the measurement, the data is ready for processing or is forwarded to a PC for further handling. A special merit is the parallel processing of the signals of several shifted antennas. So you can obtain a spatial and temporal copy of the signal distribution under identical constrains.

7. SUMMARY

We have presented a development platform which simplifies the design cycle of a MIMO software defined radio. It comprises a multi channel receiver and a MIMO channel simulator for evaluation of MIMO algorithms.

Highly flexible DSP boards featuring a synergetic combination of DSP/FPGA processing on the one hand, powerful data communication and elaborate system architecture on the other hand result in a platform offering highest performance and a vast field of functionalities.

The support of rapid prototyping and the integration of standard simulation tools make this development platform a comfortable tool which definitely speeds up simulation of MIMO algorithms.

The channel simulator of the platform delivers dependable, unlimited in time and reproducible real time channel simulations. It is suitable for testing and evaluation of MIMO receivers in real time. It models radio environments in the lab and releases the developer from the need of time consuming field tests.

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